Isolated DC/DC controller IC

Built-in Secondary-side Driver with Synchronous Rectification Active Clamp PWM Controller

BD8325FVT-M

●General Description

BD8325FVT-M is a PWM controller intended for Active clamp, current-mode isolated switching regulator.
This controller provides control outputs for driving primary-side MOSFET, and outputs with adjustable delay, which can be used for driving synchronous rectifier MOSFET on the secondary-side.
Its maximum input voltage is 20V. External startup regulator can be set at high voltage.

●Applications

- High efficiency/ large current isolated DC/DC (VINmax=100V)
- Cellular base station
- Industrial power supplies
- Car application
- 10W to 700W SMPS

●Package

	W(Typ) x D(Typ) x H(Max)
TSSOP-B30	10.00mm x 7.60mm x 1.00mm

●Features

- Ideal for Active Clamp /Rest Forward/Flyback converter
- Current-mode Control with Dual Mode Over-Current Protection
- Synchronization to External Clock
- Programmable Dead-Time (Turn-On/Turn-Off) between MAIN and AUX MOSFET by External Resistor
- Have Control Outputs for Driving Primary Side MOSFET; Have Outputs with Adjustable Time for Driving Synchronous Rectifier MOSFET in Secondary Side (OUT2F, OUT2R pin)
- Programmable Oscillator Frequency and Maximum Duty Cycle by External Resistor
- Programmable Soft-Start Time by External Capacitor
- Programmable Slope Compensation by External Resistor
- A Variety of Protection
  First Over-Current Protection (Pulse-by-Pulse mode)
  Second Over-Current Protection (HICCUP mode)
  VCC_UVLO (Input Under-Voltage Protection)
  LINE_UVLO (Line Under-Voltage Protection)

●Typical Application Circuits

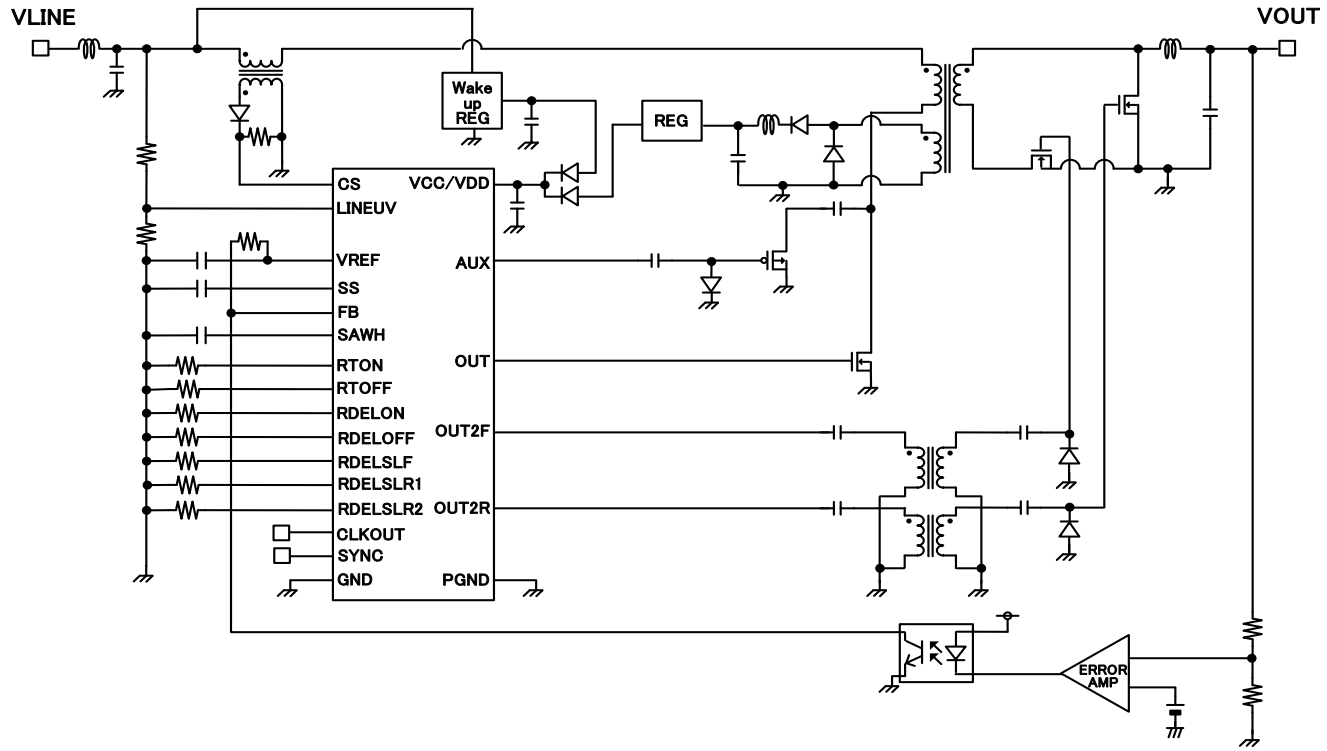


Fig.1 Typical Application Circuit

○Structure : Silicon Monolithic Integrated Circuit ○This product has no designed protection against radioactive rays.

● Pin Configuration

(TOP VIEW)

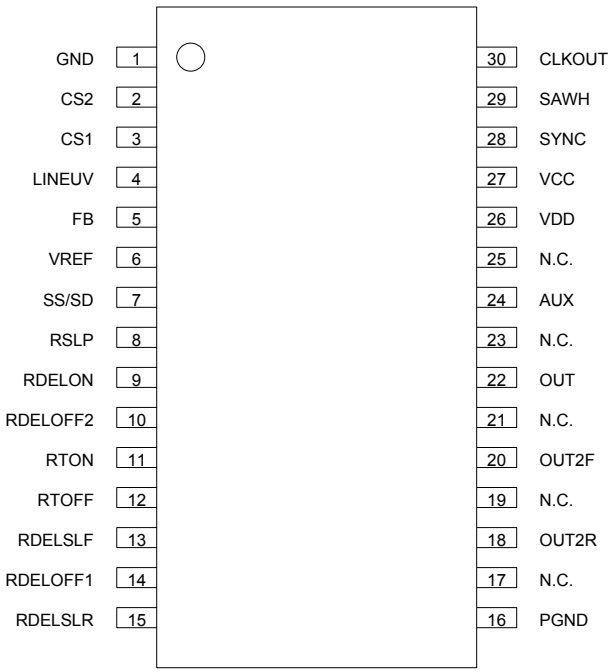


Fig.2 Pin Configuration (TOP VIEW)

●Pin Description

No	Symbol	Description	No	Symbol	Description
1	GND	GND pin	16	PGND	PWR GND
2	CS2	HICCUP mode OCP detecting pin	17	N.C	N.C
3	CS1	Current feedback & pulse-by-pulse OCP detecting pin	18	OUT2R	Gate control pin for driving freewheel NMOS in secondary side
4	LINEUV	UVLO detecting pin	19	N.C	N.C
5	FB	Feedback voltage input pin	20	OUT2F	Gate control pin for driving forward NMOS in secondary side
6	VREF	5V regulator output pin	21	N.C	N.C
7	SS/SD	Soft-Start time set pin	22	OUT	Gate control pin for driving MAIN PWM NMOS in primary side
8	RSLP	Slope compensation ramp set pin	23	N.C	N.C
9	RDELON	OUT rise/fall timing set pin	24	AUX	Gate control pin for driving active-clamp PMOS in primary side
10	RDELOFF2	AUX fall timing set pin	25	N.C	N.C
11	RTON	Switching frequency and ON time set pin	26	VDD	Power pin of FET driver
12	RTOFF	Switching frequency and OFF time set pin	27	VCC	Power pin of IC controller block
13	RDELSLF	OUT2F rise/fall timing set pin	28	SYNC	Synchronization signal input pin
14	RDELOFF1	AUX rise timing set pin	29	SAWH	Triangular wave amplitude set pin
15	RDELSLR	OUT2R rise timing set pin	30	CLKOUT	CLK output pin

●Block Diagram

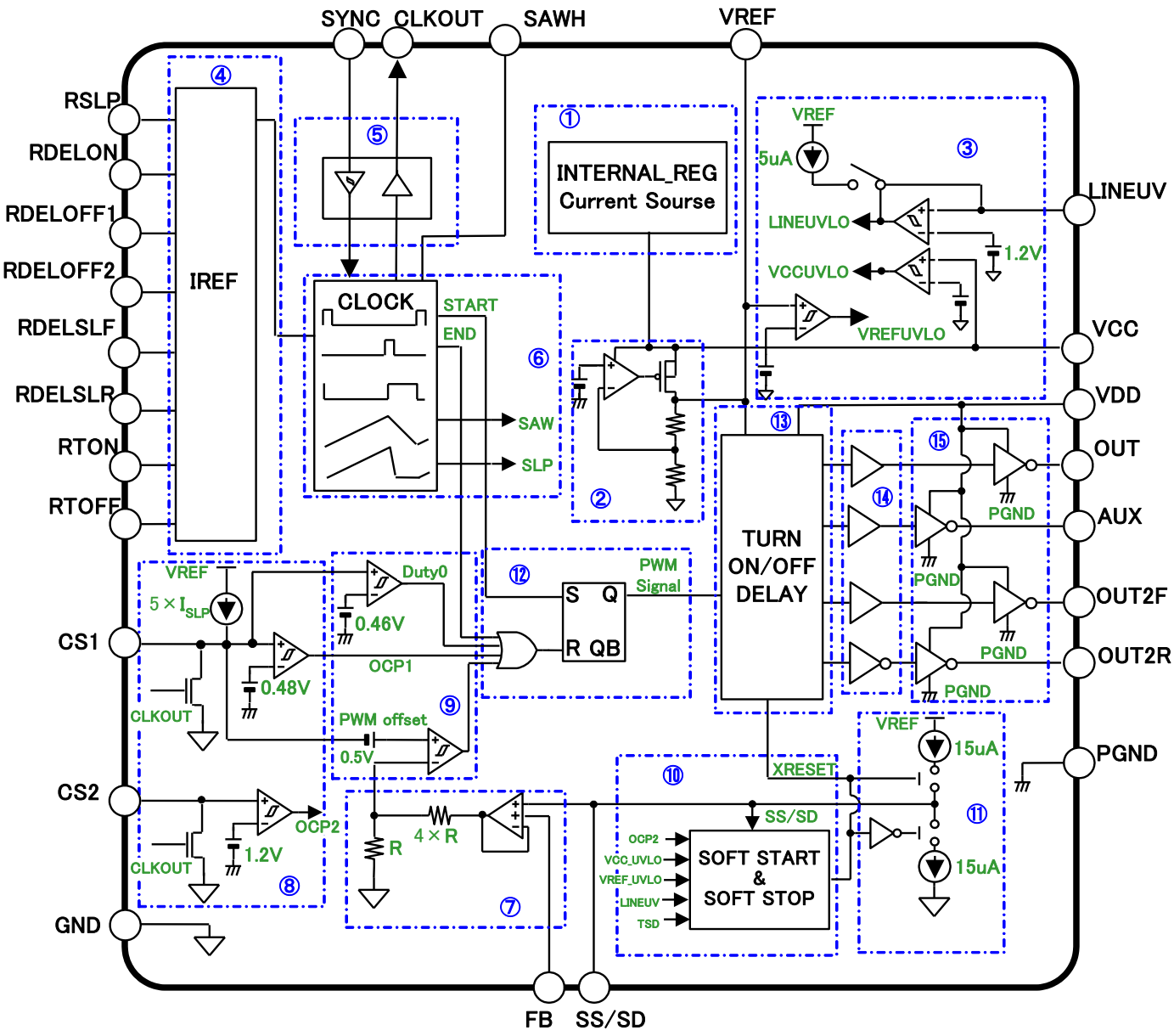


Fig.3 Block Diagram

●Description of Blocks

①Internal Power Supply

This is a regulator for powering the internal circuits via VCC. There is no direct output pin from this block.

②LDO Block

This is the 5V regulator that can provide the power supply for startup block. It should be bypassed by 0.1uF~0.47uF for stability. The circuit is utilized for the pull-up power supply of FB pin and the power supply for SAWOSC, CLK and SS/SD block. UVLO function is built-in (4.5V Typ). Once UVLO signal is detected, OUT, AUX, OUT2F and OUT2R pins turn L, and the capacitor connected to SS/SD pin is also discharged instantaneously. The short current between VREF and GND is 12mA (Typ).

③UVLO block

This is UVLO detection circuit of VCC, LINE and LDO.
The IC starts up and shuts down based on the sequence on timing chart.
When LINE UVLO signal is reset, 5uA current flows through LINEUV pin while when LINE UVLO is detected, the current is 0uA. It is possible to adjust the HYS value through the external resistor. Moreover, VCC and VREF's UVLO comparators have built-in minimum of 2us noise filters for avoiding error detection.

④Timing Set Block

For simplicity of application, the adjustable function can be achieved through external resistor:

- switching timing of OUT, AUX, OUT2F and OUT2R pin
  → resistors connected from RDELON, RDELOFF1, RDELOFF2, RDELSLF, RDELSLR pin (1.6V typ) to ground
- oscillator frequency and MAX Duty
  → resistors connected from RTON and RTOFF pin (1.6V typ) to ground
- slope compensation amplitude
  → resistor connected from RSLP pin (maximum value of sawtooth wave: 2.5V (typ)) to ground

There is a built-in open detection function such that when it is activated, the outputs are terminated. This is to avoid the pin opening caused by the incorrect mounting of external resistor.

⑤Synchronization CLK transmitter

When multiple ICs will be use, the synchronization function is implemented so that the frequency remains synchronous. The master IC provides CLKOUT signal to the slave IC through SYNC pin, and in turn, the slave IC and master IC's frequency can be synchronized. The transmitter includes the I/O part of CLK and SYNC pin. By means of extracting the frequency (at the rising edge) only, the MaxDuty can be set. There is H-side and L-side resistors connected to CLKOUT pin with a value of 0.6kΩ.

⑥SAWOSC block

The circuit is used for generating clock, duty and slope signal. In the stand-alone operation (external synchronization inactivated) the voltage of SAWH pin, which determines the amplitude of internal triangular wave, is 2.65V (typ). During the external synchronization operation, the internal circuits control the SAWH voltage to synchronize with the external clock. LVP circuit is applied to SAWH pin, and the detection and reset voltage are 1.35V (typ) and 2.6V (typ). As soon as SAWH LVP signal is detected, OUT, AUX, OUT2F and OUT2R turn L and SS/SD is discharged instantaneously, and SAWH is pre-charged (10kΩ).

⑦Feedback block

The voltage of SS/SD from block ⑪ is compared with FB voltage; the lower voltage enters the PWM signal generator.

⑧CS1, CS2 control block

This is the block intended for OCP detection.
When CS1 exceeds 0.48V, OCP1 signal is produced and RESET flag of Latch circuit (⑫) is activated. In addition, OUT=L, AUX=L, OUT2F=L, OUT2R=H and the power transfer from input to output is terminated momentarily. When the CLK enters into next cycle, the power transfer starts again. As the new cycle starts, the low-side NMOS switch connected to CS1 pin is ON when CLKOUT=H in order to make sure that the reset signal is removed. With the series of action, pulse-by-pulse mode OCP protection is observed as shown in the example application design.
When CS2 voltage exceeds 1.2V (typ), OCP2 signal is detected, the IC enters into SOFT_STOP mode and SS/SD pin starts to be discharged with 15uA current. As CS2 voltage drops to 1.2V (typ) and SS/SD≦ 0.5V, the IC returns to SOFT_START mode and starts up. Like CS1, the low side NMOS switch connected to CS2 is ON when CLKOUT=H. As shown in the example application design, if the output is shorted to ground, then the SOFT_START mode and SOFT_STOP mode alternate, the chip's HICCUP OCP protection operates.

⑨PWM signal generator

Through the comparator, CS1 related signal is compared with the lower voltage of SS/SD（⑦）and FB pin, and RESET signal for Latch circuit (⑫) is produced. To be precise, the CS1 level +0.5V and the lower of SS/SD and FB level's 1/5 are compared and the output pulse is entered into Latch circuit. In addition, when FB is lowered and SS/SD drops to 2.3V (typ), Duty0 signal turns H and RESET signal continues outputting, switching is terminated and Duty is turned to 0%. Once the switching restarts, Duty0 will not turn H unless the voltage drops to the hysteresis voltage, 2.225V (typ).

⑩RESET condition generator

According to the outputs from each protection circuit, the block controls the signal as shown below:

(1) SS/SD 15uA charge, 15uA discharge, instantaneous discharge
(2) PWM signal（OUT, AUX, OUT2F, OUT2R）OFF

⑪SS charge/discharge controller

According to whether the protection operation is detected, the operation is shown as (1) ～ (3)

(1) 15uA Charge (SOFT_START) condition: when VCC UVLO, VREF UVLO, LINE UVLO, TSD, CS2, SAWH LVP and external R-OPEN protections are not detected. SS/SD is clamped to VREF5V level.
(2) 15uA Discharge (SOFT_STOP) condition: when LINE, TSD and CS2 protections are detected. Once detected, the signal is latched. The IC will not restore to SOFT START mode unless SS/SD is 0.5V.
(3) Instantaneous Discharge (discharge resistor R=0.5kΩ) condition: when VCC UVLO, VREF UVLO, SAWH LVP and R-OPEN protection are detected.

⑫PWM signal latch block

The reference pulse signal of each output pulse is generated by SR-Flipflop.
SET: internal clock signal
RESET: PWM output signal or OCP1 signal or CLKOUT signal (Max Duty)

⑬Turn-on delay/Turn-off delay time generator

According to the dead-times, which are set by the external resistor on OUT, AUX, OUT2F and OUT2R pin in block ④, dead-times are applied to PWM signal (⑫).

⑭PREDRIVER

The level of VREF5V is shifted to VDD level.

⑮POWMOS

This is the driver's output stage for driving external MOSFET. It is constituted by NMOS and PMOS and the power supply is VDD (absolute maximum rating is 20V).

●Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Input Voltage	V_{VCC}, V_{VDD}	20	V
OUT, AUX Voltage	V_{OUT} V_{AUX}	-0.3～20	V
OUT, AUX Output Peak Current	I_{OUTH}, I_{AUXH}	2.5	A
	I_{OUTL} I_{AUXL}	2.5	
OUT2F, OUT2R Voltage	V_{OUT} V_{AUX}	-0.3～20	V
OUT2F, OUT2R Output Peak Current	I_{OUT2FH}, I_{OUT2RH}	1	A
	I_{OUT2FL}, I_{OUT2RL}	1	
Pin Voltage 1	V_{pin1} ＊1	-0.3～7	V
Pin Voltage 2	V_{pin2} ＊2	-0.3～20	V
Power Dissipation	Pd	1400 *3	mW
Operating Temperature	Topr	-40 ～ 105	℃
Storage Temperature	Tstg	-55 ～ 150	℃
Junction Temperature	Tjmax	150	℃

*1 Vpin1 applicable pin：RDELON, RDELOFF1, RDELOFF2, RDELSLF, RDELSLR, RTON, RTOFF, RSLP, VREF, CLKOUT, SAWH, FB, SS/SD, CS1, CS2, SYNC, LINEUV.
*2 Vpin2 applicable pin：VCC, VDD, OUT, AUX, OUT2F, OUT2R
*3 ROHM standard board (see below)
Derate by 11.2mW /°C when operating over 25°C

●Operating Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{VCC}、V_{VDD}	8	—	18	V
Power supply bypass capacitor	C_{VCC}	4.7	—	—	μF
Oscillator frequency set resistor (f=250kHz, 66.6% Duty)	R_{TON}	36	120	750	kΩ
	R_{TOFF}	36	120	750	kΩ
Delay time set resistor	R_{DEL}	20	120	750	kΩ
RSLP resistor	R_{SLP}	43	62	150	kΩ
Frequency range	F_{OSC}	50	—	500	kHz
VREF phase compensation capacitor	C_{REF}	0.1	—	0.47	μF
SAWH output capacitor	C_{SAWH}	0.1	—	1.5	μF
LINEUV voltage	V_{LINEUV}	—	—	5.5	V

●Electrical Characteristics

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
OVERALL						
ICC before start up	$V_{CC}<V_{UVLO}$, V_{CC}=7.5V	$I_{STARTUP}$	−	1	2	mA
ICC when normal	V_{VCC}=12v, V_{FB},$V_{CS1,CS2}$=0V Outputs not switching	I_{DD}	−	3	6	mA
VCC UVLO						
UVLO Reset voltage		$V_{UVLOOFF}$	8.1	8.5	8.9	V
UVLO Hysteresis		ΔV_{UVLO}	0.2	0.5	0.8	V
LINE UVLO						
LINE UV threshold voltage		V_{LINEUV}	1.176	1.200	1.224	V
LINE UV hysteresis current		I_{LINEUV}	-5.5	-5	-4.5	µA
SOFT_START/SOFT_STOP						
SS charge current		I_{SSC}	-16.8	-15	-13.2	µA
SS discharge current		I_{SSD}	13.2	15	16.8	µA
VREF output						
VREF voltage (1)	T_J=25℃	V_{REF1}	4.85	5.00	5.15	V
VREF voltage (2)	0A＜I_{REF}＜5mA over temperature	V_{REF2}	4.75	5.00	5.25	V
VREF short current	VREF=0V, T_J=25℃	I_{SC}	-21	-12	-6	mA
Reference Voltage 1 for set pin	*1	V_{REFR1}	1.544	1.6	1.656	V
Reference Voltage 2 for set pin	*2	V_{REFR2}	1.2	1.6	2.0	V
INTERNAL SLOPE COMPENSATION（RSLP）						
RSLP pin max voltage	RSLP=RTON=RTOFF=120kΩ	V_{RSLPH}	2.25	2.5	2.75	V
OSCILATOR／PWM						
Oscillator frequency	T_J=25℃	F_{OSC}	237	250	265	kHz
（RTON = RTOFF = 120kΩ）	-40℃<T_J<105℃, 8V<VCC<18V	F_{OSC2}	225	250	270	kHz
PWM MAX Duty	RTON = RTOFF = 120kΩ	Dmatch	63.1	66.6	70.1	%
SYNC function						
SYNC input current	SYNC=5V	I_{SYNC}	−	10	15	µA
SYNC input High voltage		V_{SYNCH}	3	−	5.5	V
SYNC input Low voltage		V_{SYNCL}	−	−	0.5	V
CLKOUT output H-side ON Resistance	Iout = ±100uA	$R_{CLKOUTH}$	−	0.6	2	kΩ
CLKOUT output L-side ON Resistance		$R_{CLKOUTL}$	−	0.6	2	kΩ
SAWH output voltage	SYNC=0V	V_{SAWH}	2.45	2.65	2.85	V

*1 Correspond to RDELON, RDELOFF1, RDELOFF2, RDELSLF, RDELSLR.
*2 Correspond to RTON, RTOFF. LIMIT is wider than *1.

●**Electrical Characteristics**

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
CURRENT SENSE						
Duty0 Reset Threshold Voltage	FB sweep up	V_{DUTY0A}	0.083 * VREF	0.092 * VREF	0.101 * VREF	V
Duty0 Detection Threshold Voltage	FB sweep down	V_{DUTY0B}	0.08 * VREF	0.089 * VREF	0.098 * VREF	V
CS1 Level Shift Voltage		V_{LVL}	0.09 * VREF	0.1 * VREF	0.110 * VREF	V
Current Limit Voltage (1) Cycle-by-Cycle		V_{CS1}	0.087 * VREF	0.096 * VREF	0.105 * VREF	V
Current Limit Voltage (2) Hiccup mode		V_{CS2}	0.216 * VREF	0.24 * VREF	0.264 * VREF	V
OUTPUT (For driving Primary side FET, applied to OUT, AUX pin)						
H-side ON Resistance	I_{OUT}= -200mA ,VDD=10V	R_{MSOH}	—	1	1.5	Ω
L-side ON Resistance	I_{OUT}=+200mA ,VDD=10V	R_{MSOL}	—	1	1.5	
OUTPUT (For driving secondary side FET, applied to OUT2F, OUT2R pin)						
H-side ON Resistance	I_{OUT}= -100mA ,VDD=10V	R_{SROH}	—	1.6	2.90	Ω
L-side ON Resistance	I_{OUT}=+100mA ,VDD=10V	R_{SROL}	—	1.50	2.70	
OUTPUT Delay time						
Delay time 1 (OUT2R_off to OUT_on)	C_{LOAD}=1000pF, R_G=3.6Ω R_{DELON}=120kΩ	T_{RDELON}	87	175	263	ns
Delay time 2 (OUT2R_off to AUX_off)	C_{LOAD}=1000pF, R_G=3.6Ω $R_{DELOFF1}$=120kΩ	$T_{RDELOFF1}$	17	35	53	ns
Delay time 3 (OUT_off to AUX_on)	C_{LOAD}=1000pF, R_G=3.6Ω $R_{DELOFF2}$=120kΩ	$T_{RDELOFF2}$	60	120	180	ns
Delay time 4 (OUT2R_off to OUT2F_on)	C_{LOAD}=1000pF, R_G=3.6Ω R_{DELSLF}=120kΩ	$T_{RDELSLF}$	60	120	180	ns
Delay time 5 (OUT_off to OUT2R_on)	C_{LOAD}=1000pF, R_G=3.6Ω R_{DELSLR}=120kΩ	$T_{RDELSLR}$	30	60	90	ns

●**Typical Performance Characteristics (Reference data)**

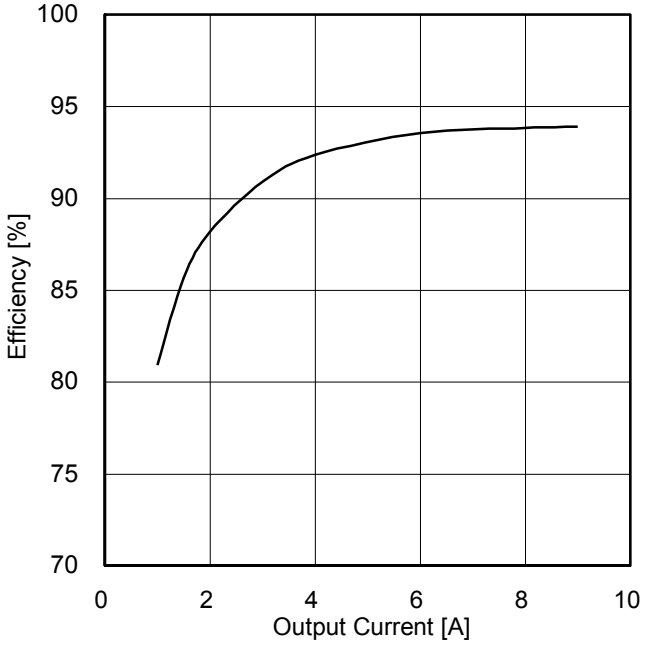


Fig.4 Efficiency-Output Current

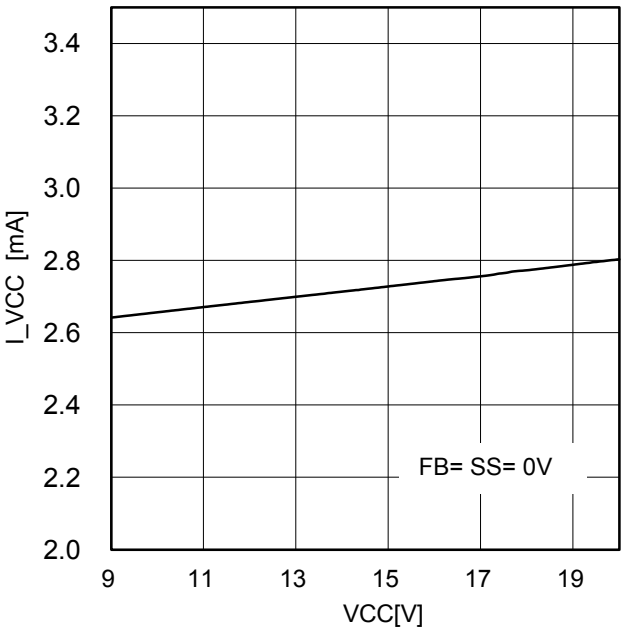


Fig.5 I_VCC - VCC

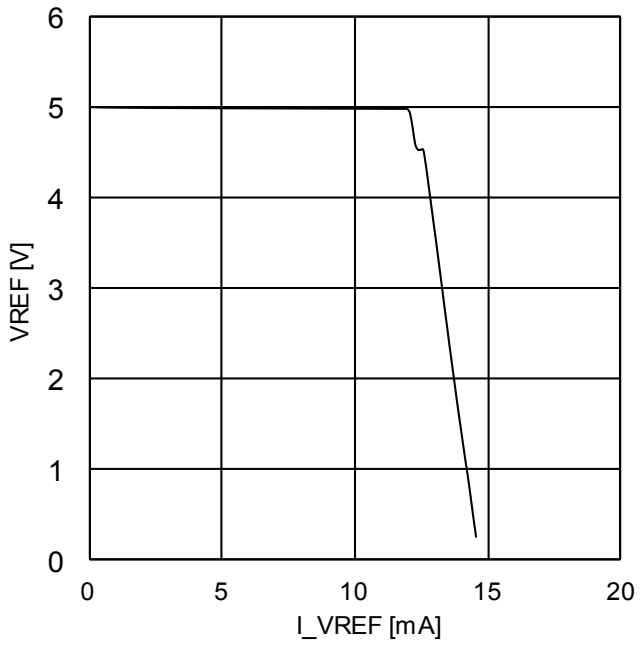


Fig.6 I_VREF - VREF

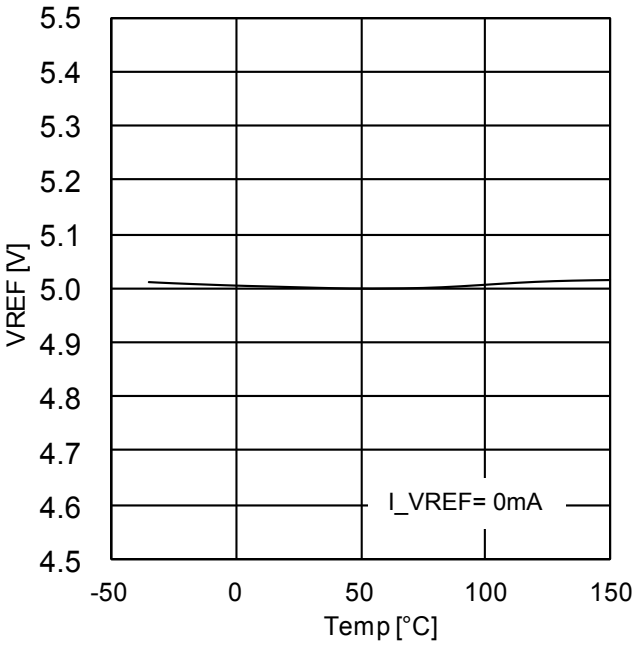


Fig.7 VREF - Temp

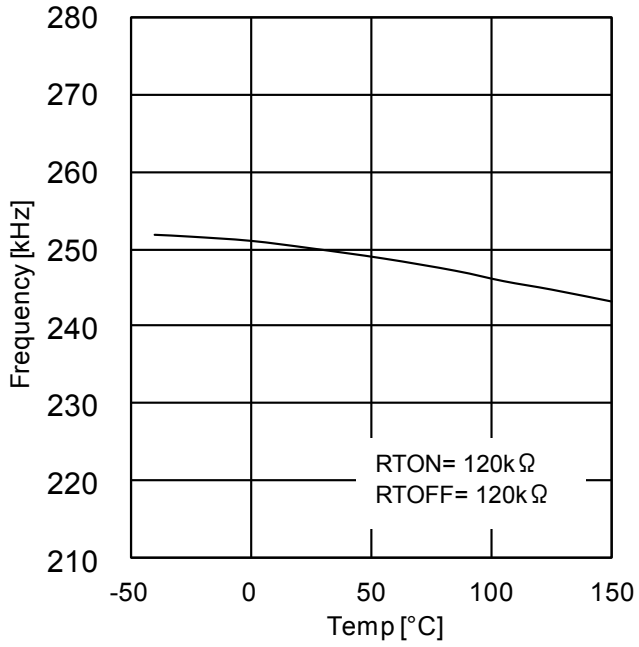


Fig.8 Frequency - Temp

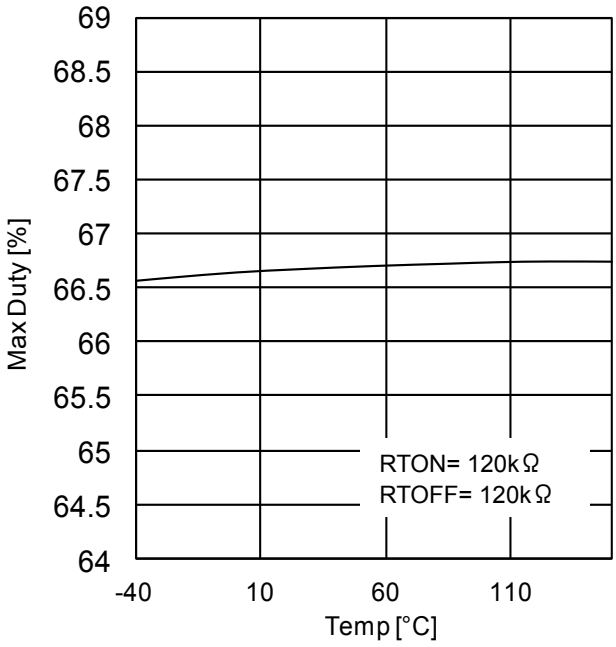


Fig.9 Max Duty - Temp

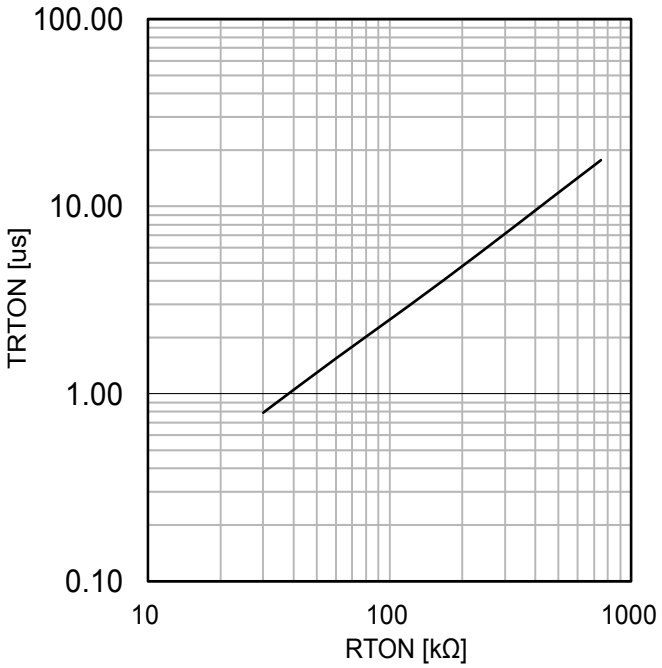


Fig.10 TRTON - RTON

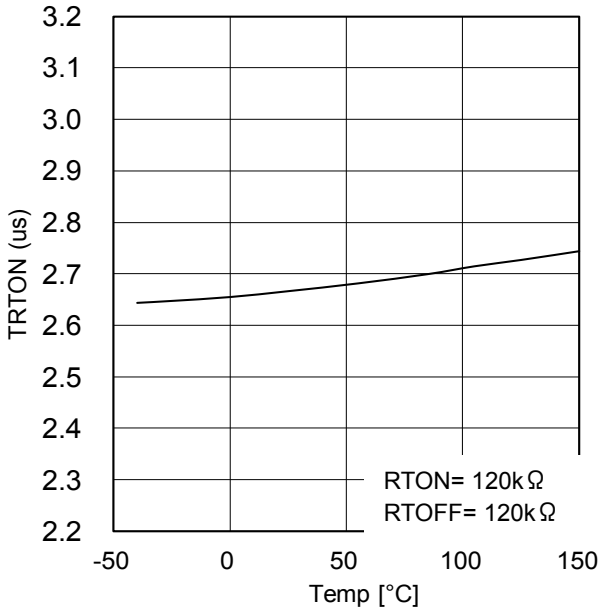


Fig.11 TRTON - Temp

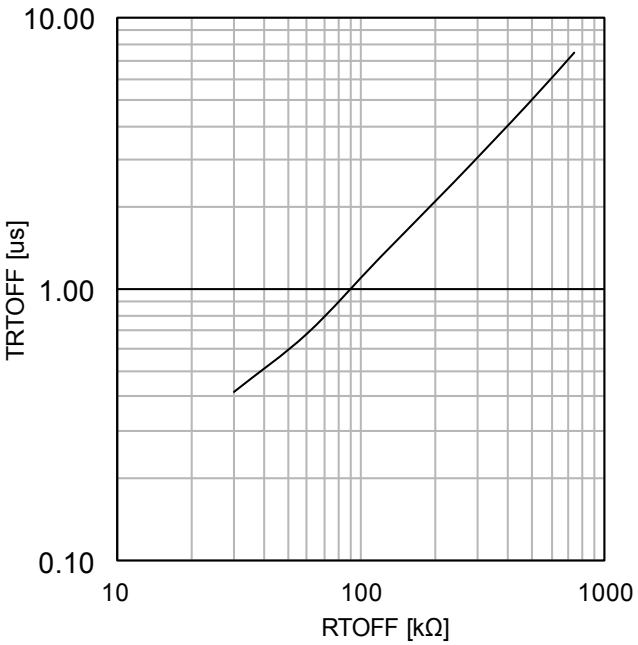


Fig.12 TRTOFF - RTOFF

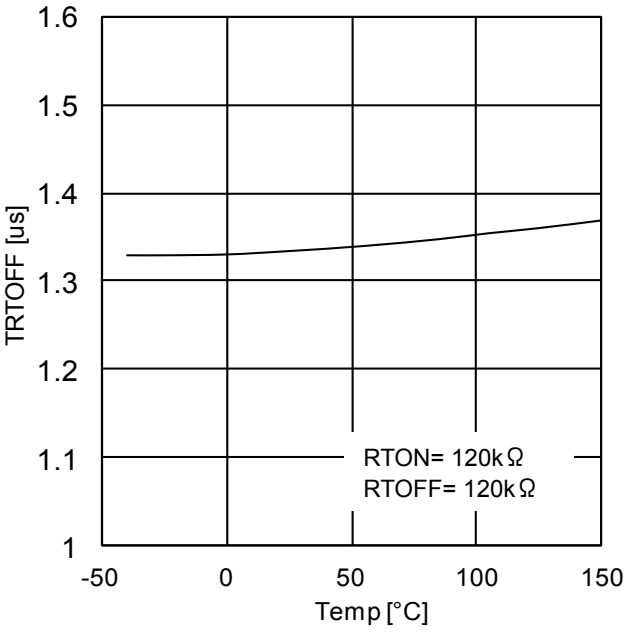


Fig.13 TRTOFF - RTOFF

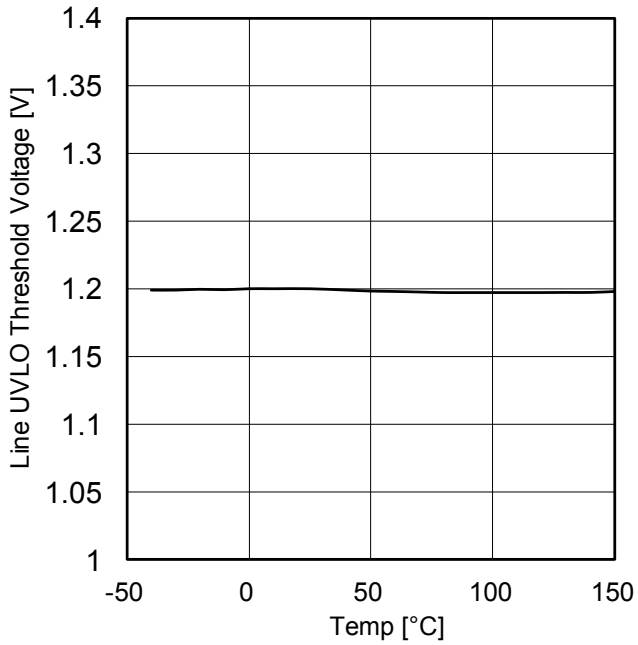


Fig.14 LINEUV Threshold - Temp

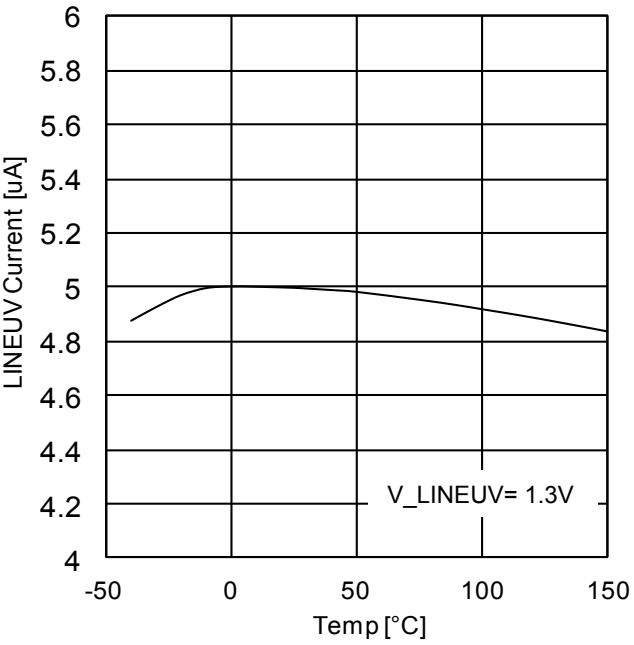


Fig.15 I_LINEUV – VLINEUV

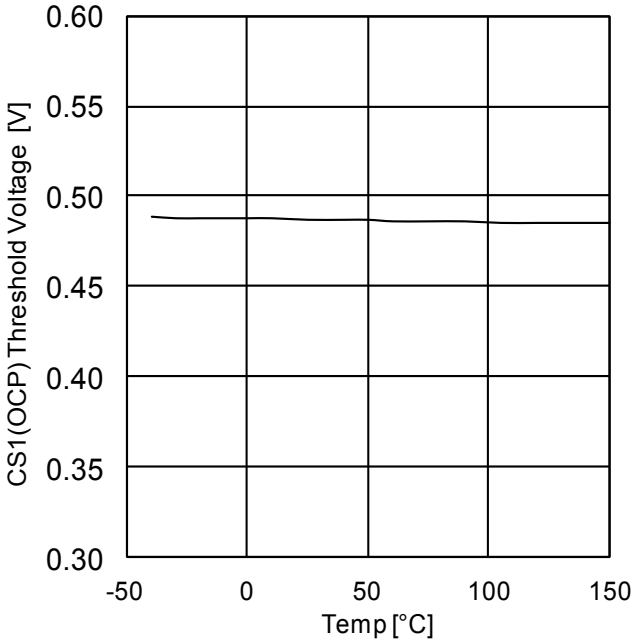


Fig.16 CS1 (OCP) Threshold – Temp

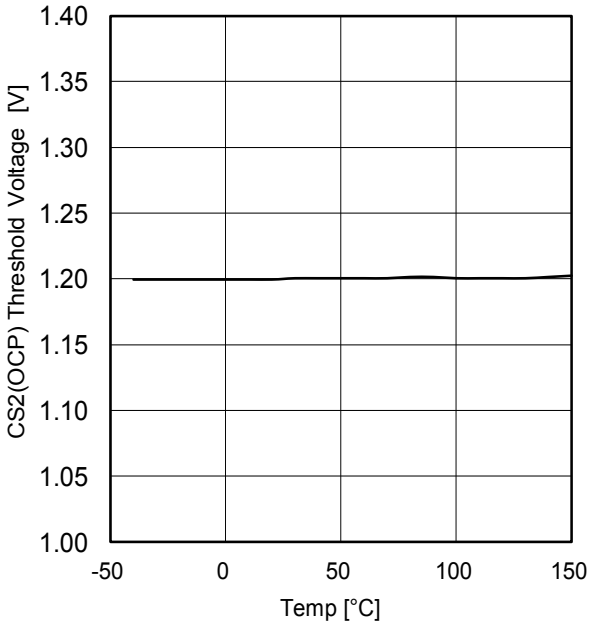


Fig.17 CS2 (OCP) Threshold - Temp

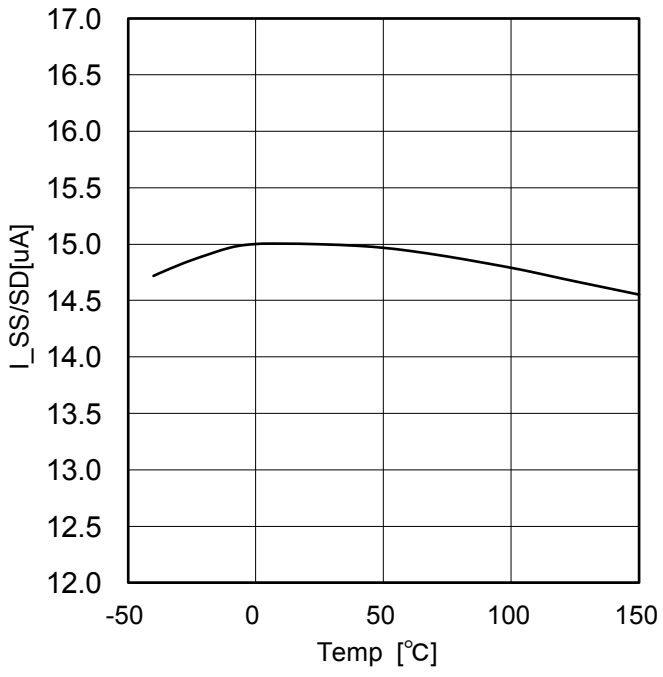


Fig.18 I_SS/SD – Temp

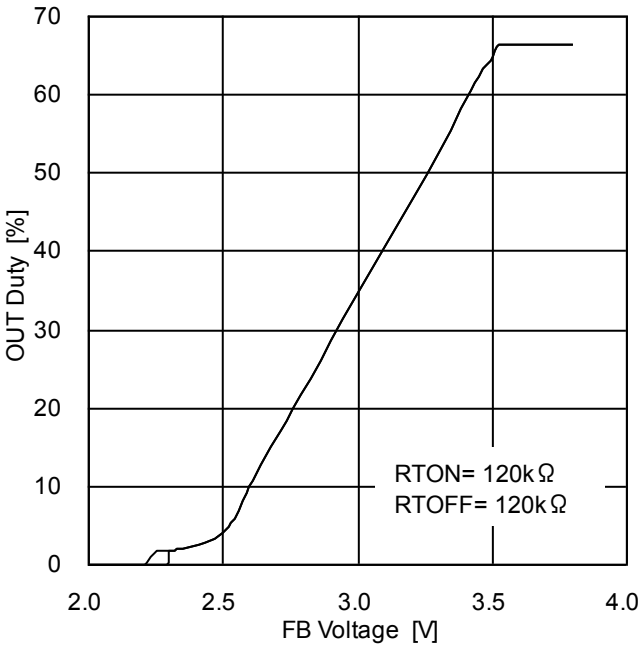


Fig.19 OUT Duty - VFB

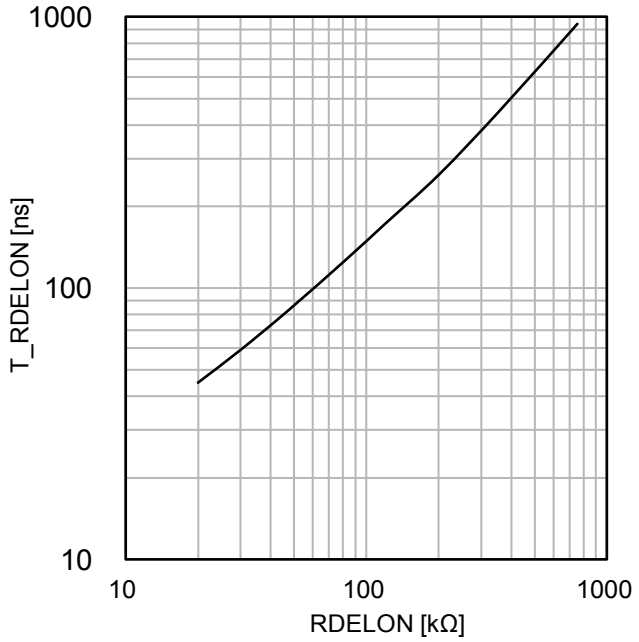


Fig.20 TRDELON - RTON

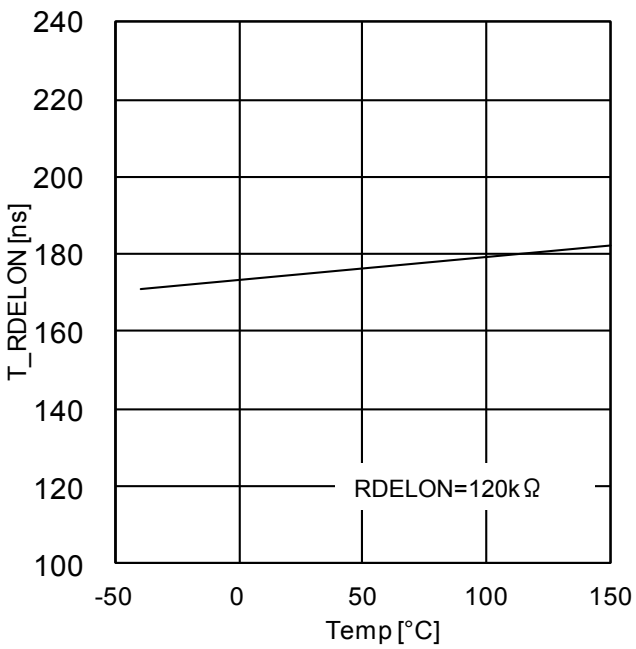


Fig.21 TRDELON - Temp

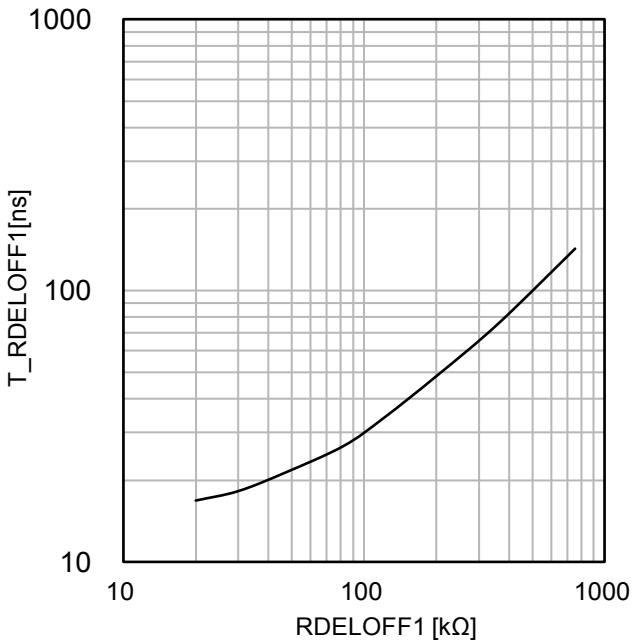


Fig.22 TRDELOFF1 – RTOFF1

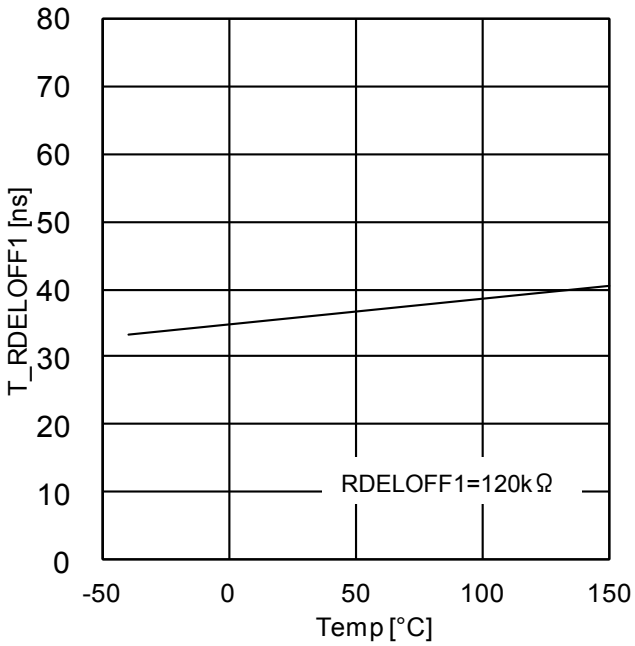


Fig.23 TRDELOFF1 - Temp

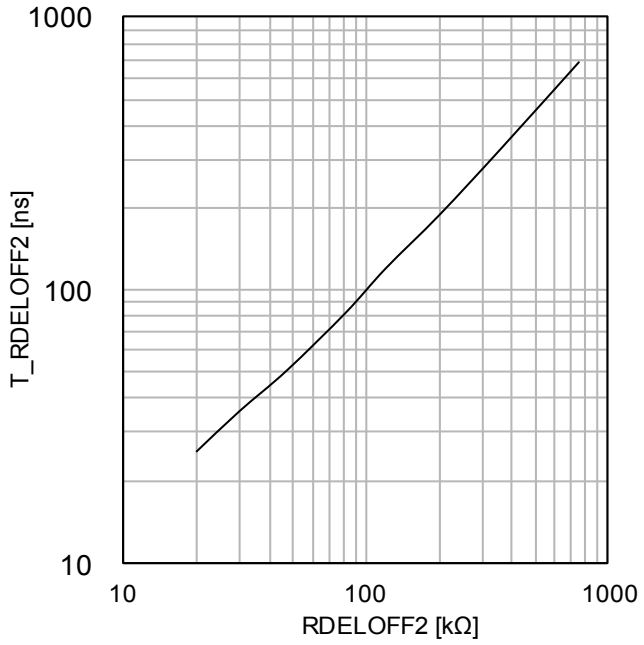


Fig.24 TRDELOFF2 – RDELOFF2

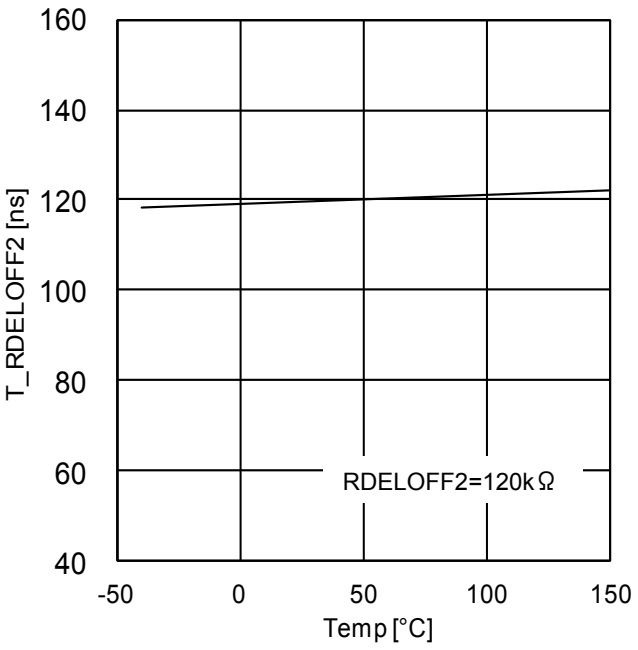


Fig.25 TRDELOFF2 - Temp

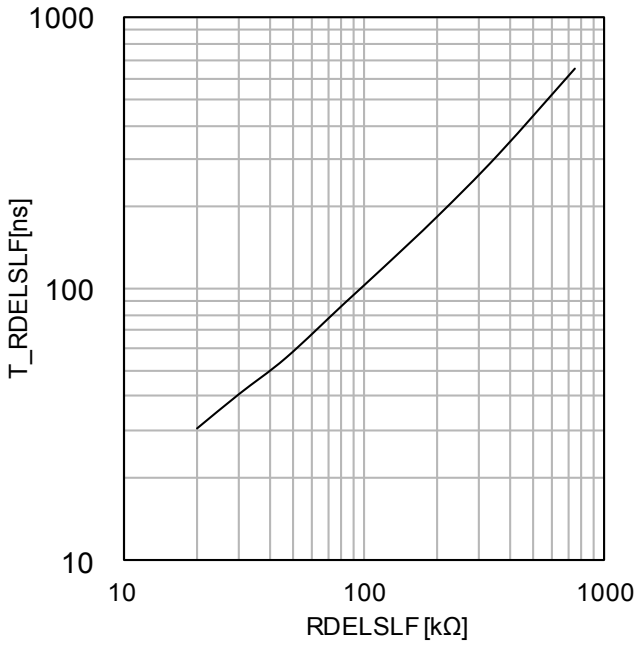


Fig.26 TRDELSLF - RDELSLF

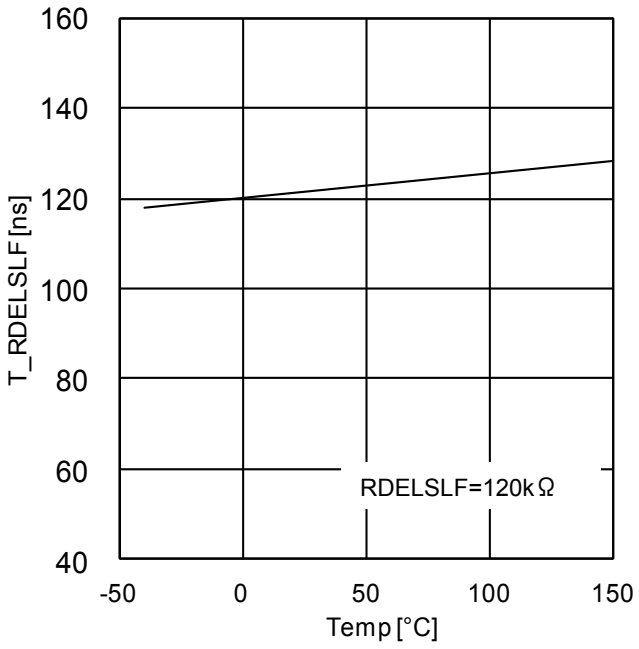


Fig.27 TRDELSLF - RDELSLF

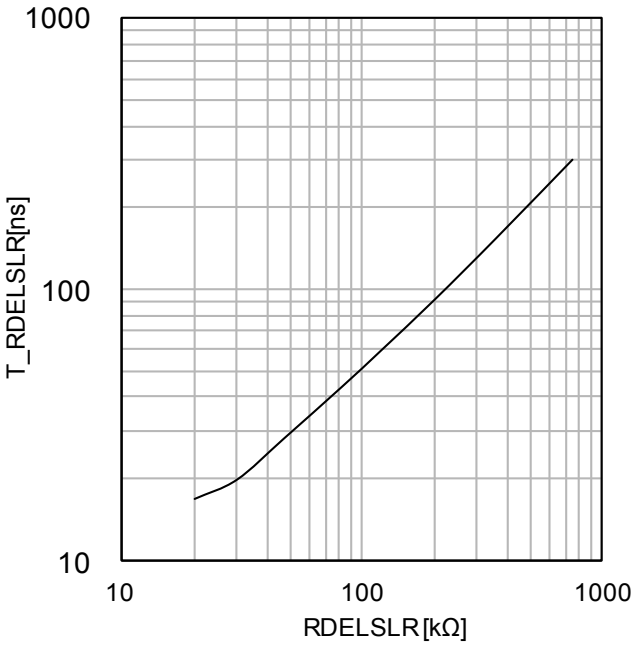


Fig.28 TRDELSLR - RDELSLR

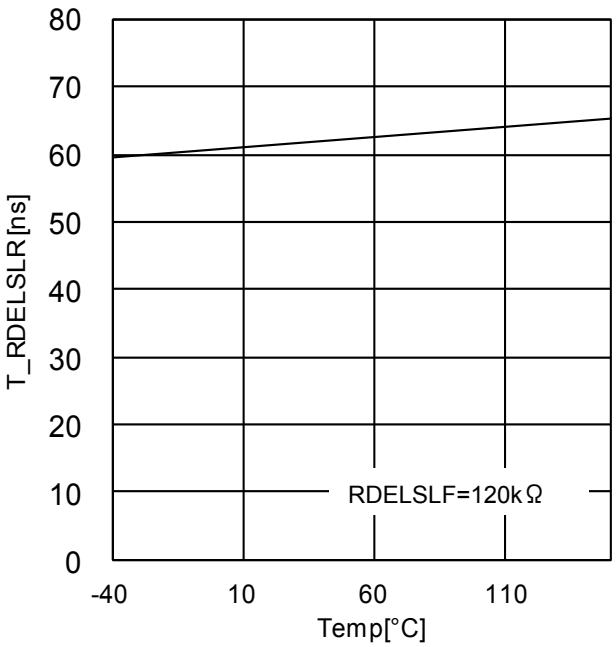


Fig.29 TRDELSLR - RDELSLR

●Functional Details and Operation

1. The setting of startup regulator

The external startup regulator is necessary in case of power supply above 18V. The output of startup regulator is assumed to be 10-12V and the min value should be above 9V.

The maximum consumed current is 4mA.

2. Handling of N.C. pin

17, 19, 21, 23, 25 pin are NC pins. As they include GND, please don't connect them to any node, just make them in floating state. Adjacent pin short protection is invalid.

3. Output signal for driving NchFET / PchFET

Regarding NchFET driving signal (OUT), active-clamp PchFET driving signal (AUX) in primary side and driving signal(OUT2F,OUT2R) in secondary side, the signals' output resistance is small and can be adjusted by external resistor so that the driving signal can be applied to multiple converter requirements. As expected, the spike noise becomes big when the external resistor is small. Please use appropriate resistor to adjust the slew rate.

4. Range of external resistor connected to adjustable pin

There are several adjustable pins connected by external resistor. The resistors (RDELON, RDELOFF1, RDELOFF2, RDELSLF, RDELSLR) can set the switching Frequency, Duty (RTON/RTOFF), Dead-time of primary and secondary side as well as the dead-time between primary side and secondary side (P.2,3). Set the above resistors in the range as shown in P.6. Take note that if the resistance is out of range, the IC may break or weaken because of open detection. The estimated formulas of switching Frequency and Max Duty are shown below:

$$TRTON \cong 22.22 \times 10^{-12} \cdot RTON$$
$$TRTOFF \cong 11.11 \times 10^{-12} \cdot RTOFF$$
$$fosc \cong \frac{1}{TRTON + TRTOFF}$$
$$MaxDuty \cong \frac{TRTON}{TRTON + TRTOFF}$$

5. Protection function

The protection functions of the IC are the following:

- ・VCC UVLO — UVLO signal will reset when VCC=8.5V and will be detected when VCC=8V. There is a 2us (min) noise filter.
- ・VREF UVLO — Once VCCUVLO signal is removed, VREF(5V) starts up. UVLO signal will reset when VREF=4.6V (typ) and will be detected when VREF=4.5V (typ). There is a 2us noise filter.
- ・LINE UVLO — It is determined by the resistance voltage divider between LINE and GND. When UVLO signal has been reset, 5uA source current flows out. The current combined with external resistor determines the hysteresis. Once LINEUV signal is detected, the IC enters into SOFT_STOP mode and SS/SD pin starts to be discharged by 15uA current. If LINEUV signal is reset and SS/SD≦ 0.5V, the IC starts up in SOFT START mode. The absolute maximum rating of LINEUV pin is 7V and its' rating of operation is 5.5V.
- ・SAWH_LVP — When SAWH < 1.35V (typ), SAWH_LVP signal is detected. The switching operation is stopped and SS/SD pin is discharged instantaneously. The external capacitor connected to SAWH pin begins to be charged quickly (several hundred mA). If the SAWH becomes 2.6V (typ), SAWH_LVP signal will reset and the quick discharge will stop, and SS/SD will start to be charged (soft start).
- ・TSD — Protects the IC from thermal runaway caused by the excessive rise of temperature. TSD (Thermal Shutdown) protection is activated when the chip's internal temperature is 170℃ and the IC restarts when the temperature drops to 150℃. Like LINE UVLO, TSD will also make the IC into SOFT STOP mode. In consideration of the power dissipation during actual use, it is necessary to consider heat design with sufficient margin. Application design should never make use of the thermal shutdown circuit.
- ・CS1, CS2 — The IC has two OCP protection modes, Pulse-by-Pulse and Hiccup. The Cycle-by-Cycle mode terminates the conduction cycle if CS1 voltage becomes 0.48V (typ). The OFF latch is reset and conduction is ON when CLKOUT=H→L in the next cycle. If the voltage on CS2 pin exceeds 1.2V (typ), the IC enters Hiccup mode protection. While in the Hiccup mode, the IC enters into SOFT START mode as well as LINEUV. If the over load condition sustains, the IC will alternate between SOFT START mode and SOFT STOP mode. If Hiccup mode will not be used, CS2 pin should be shorted to GND pin.
- ・R_OPEN — When the pins of RTON, RTOFF, RDELON, RDELOFF1, RDELOFF2, RDELSLF, RDELSLR, RSLP are OPEN, the protection is activated. OUT, AUX, OUT2F, OUT2R stop switching instantaneously (L level) and the capacitor connected to SS/SD pin is discharged instantaneously.

6. Operation of SS/SD pin, VREF.

When power on — When VCCUVLO signal is reset, VREF starts up and in turn, VREF UVLO and SAWH LVP signal will also reset. If LINE UVLO, OCP and TSD signals are not detected, the capacitor connected to SS/SD pin starts to be charged (15uA typ). The voltage of SS/SD pin is clamped by VREF.

When power off — When LINEUV signal is detected, the capacitor connected to SS/SD pin starts to be discharged (-15uA).
If VCC UVLO signal is detected, VREF is discharged naturally. Besides, the rise/fall time is determined by the formula T=CV/Ichg (Idischg)

7. SOFT STOP mode

In addition to the protection condition of #6, when LINE UVLO, TSD or CS2 signal is detected, the IC enters SOFT STOP mode. During this mode, in consideration of external device and the heat caused by CS2 detection or TSD detection, OUT pin is OFF directly. However, AUX, OUT2F and OUT2R pins continue switching to avoid over-current and over-voltage to happen (refer to the timing chart). Moreover, SS/SD pin is discharged by 15uA current, and the Duty of AUX, OUT2F, OUT2R gradually decrease as SS/SD voltage decreases. When SS/SD voltage drops to 2.215Vtyp (Duty0 is detected), AUX, OUT2F and OUT2R will stop switching. If SS/SD voltage is discharged to 0.5V and the other protections are not activated, then SS pin starts to be charged again and the output starts up in SOFT START mode automatically.

8. PWM operation

As shown in Fig.30, Slope signal is generated through CLKOUT signal, which is generated from RTON, RTOFF and SAWH voltage. The slope signal is buffered and outputted to RSLP pin. The current flowing through RSLP pin is proportional to SLOPE voltage, and in addition the current is amplified 5 times and outputted to CS1 pin. The slope current is overlapped with sensing current and converted to the voltage on external resistor RS for the stability of the peak current mode control loop. The voltage signal is shifted up by 0.5V (CS1 Level Shift Voltage) and transmitted to INP input of PWM comparator. However, the other input INN voltage is one fifth of FB_SS_L, which is the lower voltage within FB and SS pin.

If two input signals are compared and the PWM latch block's reset signal is outputted, then the PWM pulse width can be determined. If INN node voltage is above 0.46V (typ) during the sweep up of FB_SS_L, Duty0 turns H and PWM_Latch_R turns constant H (Duty=0%). Moreover, Duty0 turns H if the INN node voltage drops to 0.445V (typ) during the sweep down of FB_SS_L.

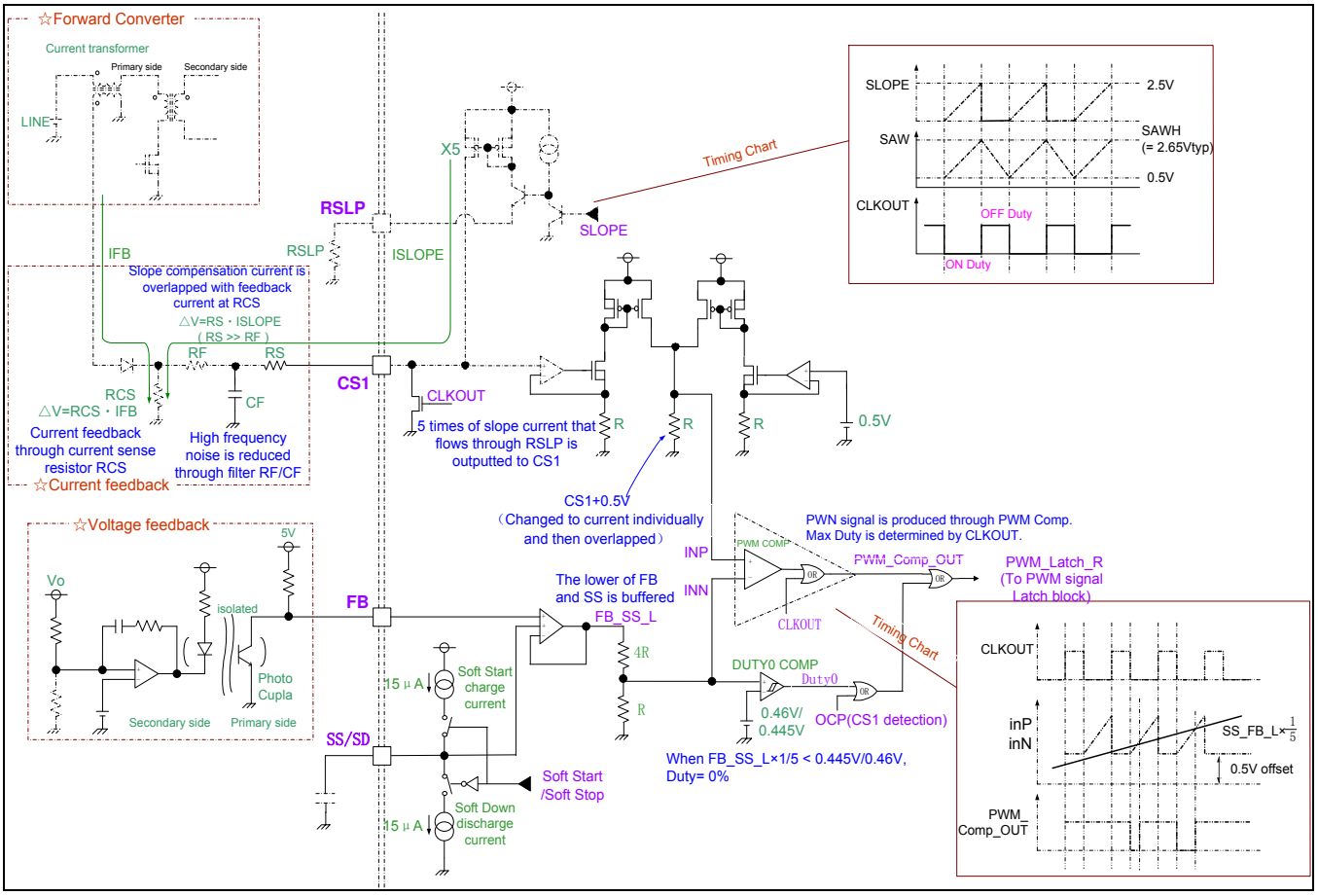


Fig.30 –Simplified Diagram of the PWM Comparator Proximity Circuit

9. Synchronization function

(1) Outline

When multiple ICs will be used, the synchronization function is implemented so that the frequency for all ICs will be the same.

The master IC provides CLKOUT signal to the slave IC through SYNC pin, and the slave IC and master IC's frequency now turn to be synchronized. The transmitter includes the I/O part of CLK and SYNC pin. By means of extracting the frequency (at the rising edge) only, the Max Duty can be set. There are H side and L side resistors connected to CLKOUT pin, and the value is 0.6kΩ.When multiples ICs will be used, the synchronization function is implemented so that the frequency remains synchronous. When the synchronization function operates, the master IC controls the slave ICs and sets their Max Duty (RTON, RTOFF) and slope compensation (RSLP). The function operates when the master IC's CLKOUT pin is connected to slave IC's SYNC pin.

Synchronization function operates when CLK signal exists on SYNC pin and returns to free running mode when CLK signal disappears. It is recommended to determine whether synchronization is needed before startup. Take note that connecting bigger capacitor to SAWH pin will reduce the jitter but prolong the settling time of synchronization. Moreover, the output may be unstable during capture course, pay attention to it when synchronization function switches or when operation of IC suddenly stops.

If the synchronization function is not needed, SYNC pin should be connected to GND and CLKOUT pin should be left open.

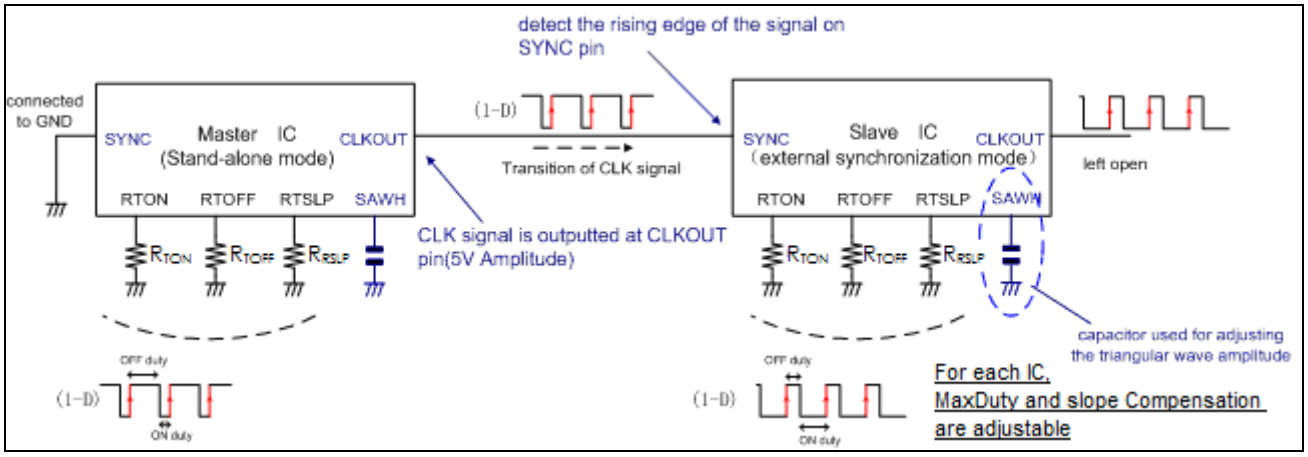


Fig.31 Connection example of external synchronization

(2) Operation setting

Frequency setting : Please set the slave IC's typical frequency within -3～+0.5% of master IC's and the external resistor that programs the frequency should be the of ±0.5% precision.

(example) master IC : RTON=RTOFF=120kΩ(fosc= 250kHz, Max Duty=66.6%) , and the Max Duty of slave IC is set at 62%

$$245.5kHz \le \frac{1}{TRTON + TRTOFF} \le 251.25kHz$$

$$MaxDuy = \frac{TRTON}{TRTON + TRTOFF} = 0.62$$

Thus, RTON=113kΩ、RTOFF=137kHz (fosc≒248.0kHz, MaxDuty≒62.3%)

Capacitor connected to SAWH : 0.1u～1.5uF ceramic capacitor

Although connecting big capacitor can reduce the jitter, it takes long time to stabilize the synchronization course.

(3) Principle of operation

The RTON (determine charge current) and RTOFF (determine discharge current) pins are used to generate SAW triangular wave, thus the switching frequency and MaxDuty can be set. The RSLP pin is used to set the slope compensation.

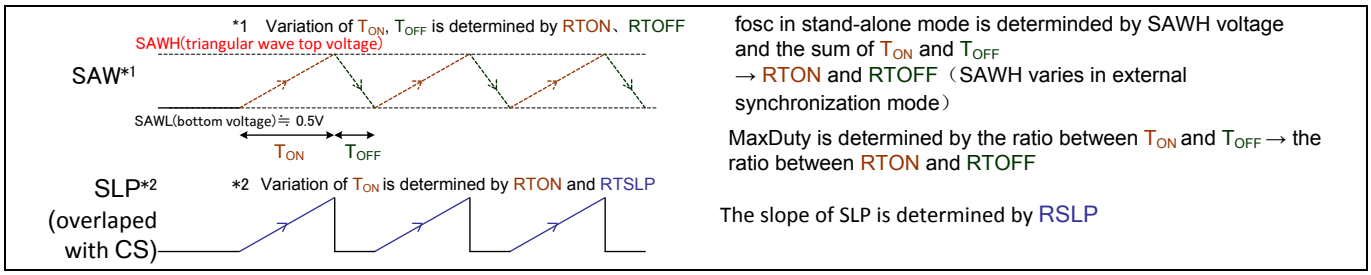


Fig.32 Principle of frequency generation

The internal frequency fosc is compared with external frequency fsync, and the difference is fed back. In this way, the synchronization like PLL is observed. If fosc＞fsync (the internal frequency fosc is faster), the capacitor connected to SAWH pin is charged through 100kΩ, and the triangular wave top voltage is leveled up. When fosc is slower, the capacitor is discharged so that fosc gets near to fsync. The capacitor connected to SAWH pin is used for smoothing the voltage variation when switching, in this way stable frequency can be outputted.

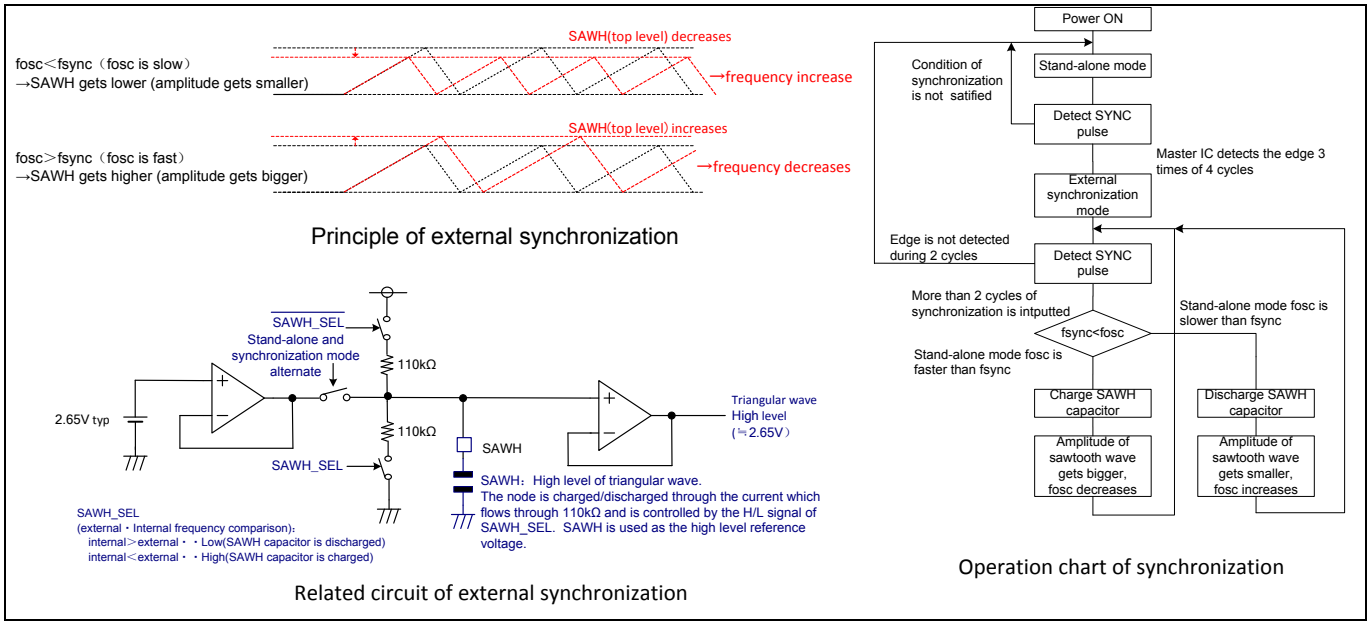


Fig.33 Principle of external synchronization

9. VCC pin and VDD pin

Connect VDD to VCC with decoupling capacitor. If the resistance is added between VCC pin and VDD pin to prevent conduction noise, use resistance less than 50Ω.

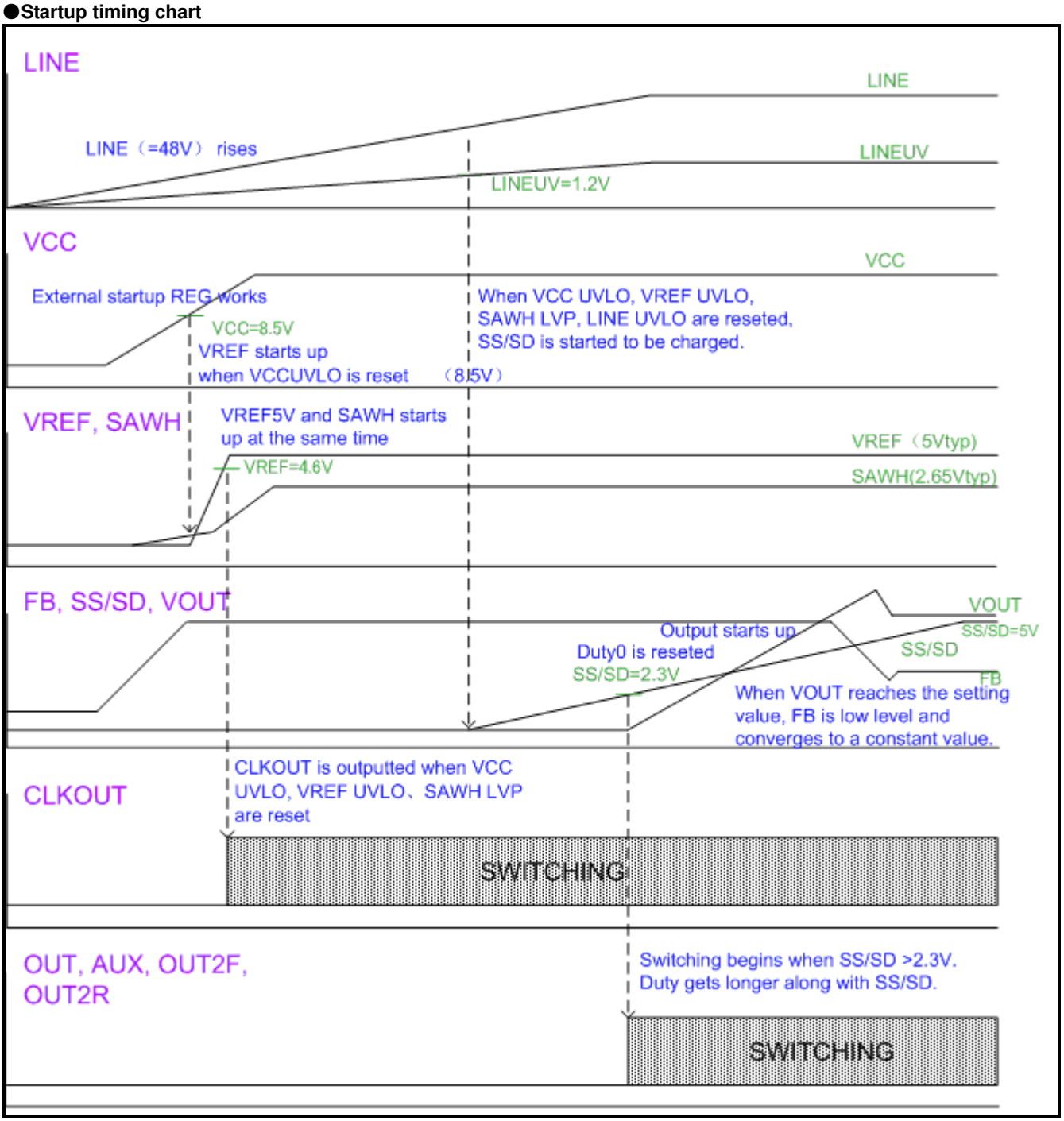
●Design of Pattern Diagram

(1) The switching voltages on the line of OUT, AUX, OUT2F, OUT2R, SYNC, CLKOUT, (SYNC) pin and the application board's switching line are the noise source. Please avoid the sensitive line of FB, LINEUV, CS1, CS2, RSLP, RDELON, RDELOFF2, RTON, RTOFF, RDELSLF, RDELOFF1, RDELSLR, SS, SAWH and VREF from being wired in parallel with noise source line. Furthermore, place the external device near the sensitive pin and the GND of external device should be connected to the low noise GND.

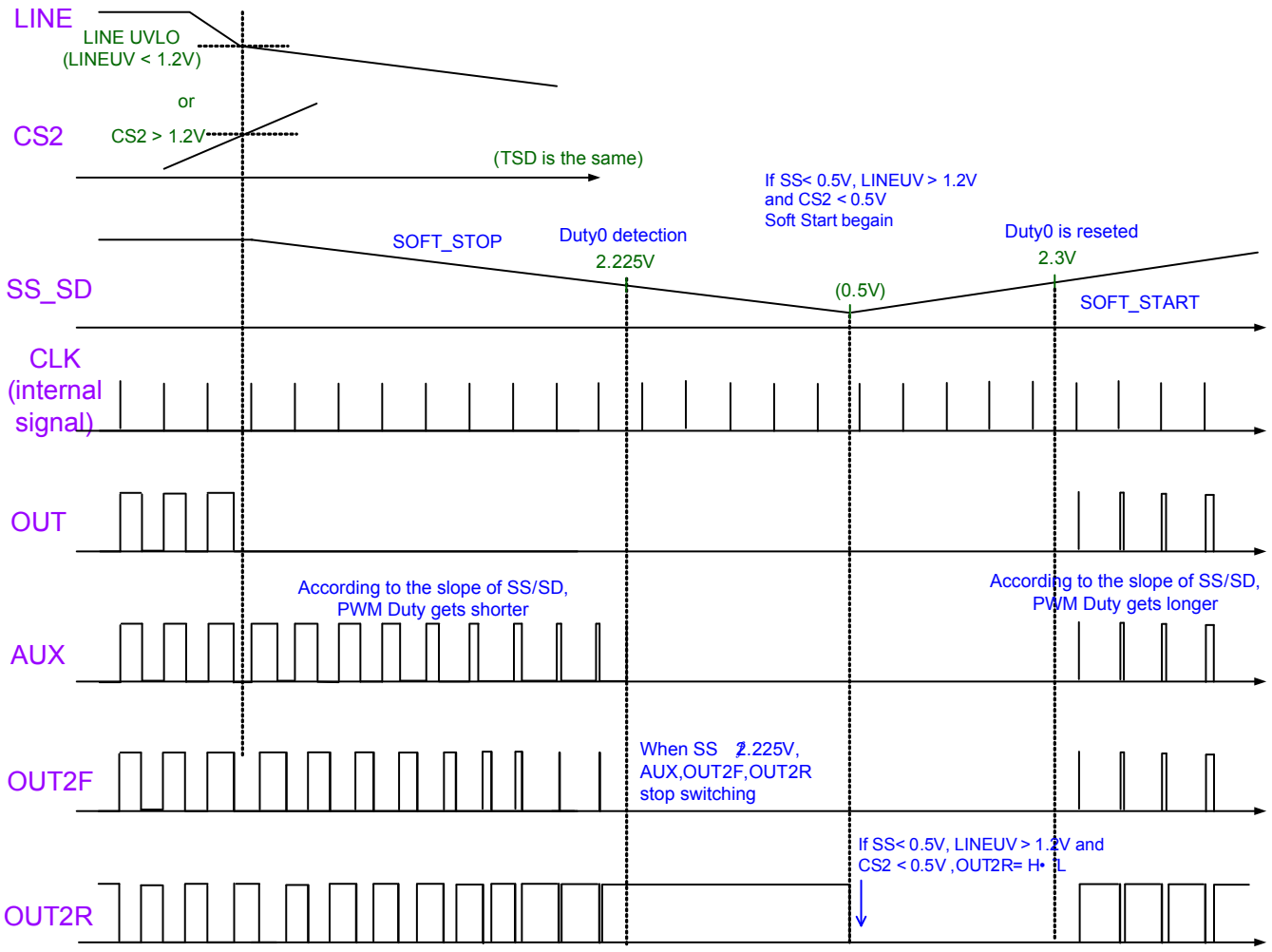
(2) For reducing the parasitic inductance of wire from OUT, AUX, OUT2F, OUT2R to FET gate line, it is better to make the wire as short as possible. Also, As switching current occurs while driving the FET gate, the current loop area should be made small.

(3) VCC is the power supply for IC internal analog circuits and it should be immune to external noise. On the one hand, VDD is the power supply for the output driver and switching noise occurs when the driver works. Therefore, VCC and VDD should not use the common input capacitor, but individual input capacitor near their pins. Additionally, the GND of input capacitor connected to VCC pin should be connected to low noise GND. Likewise; the GND pin of the IC also should be connected to low noise GND.

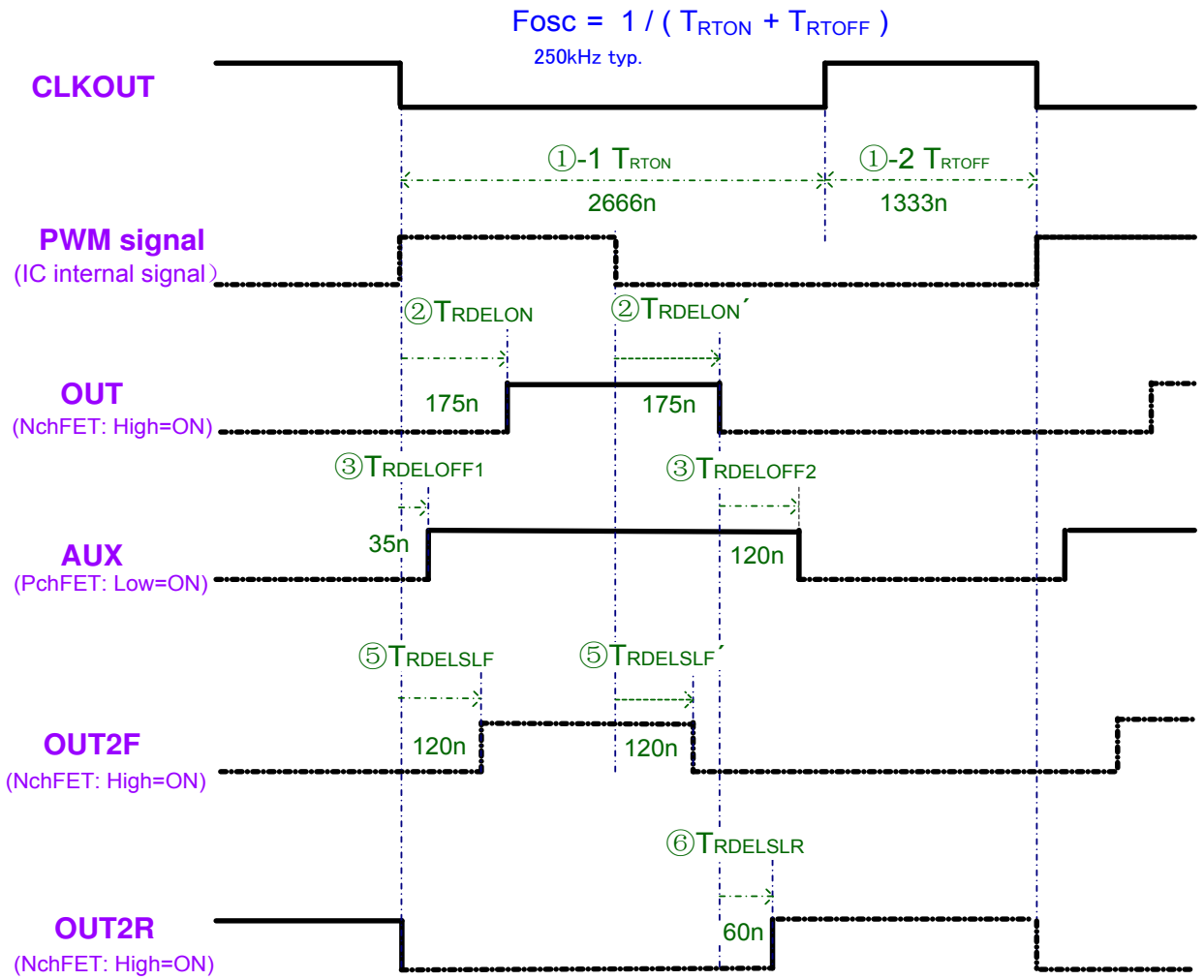
●Startup timing chart



●SOFT-STOP and Restart Timing Chart



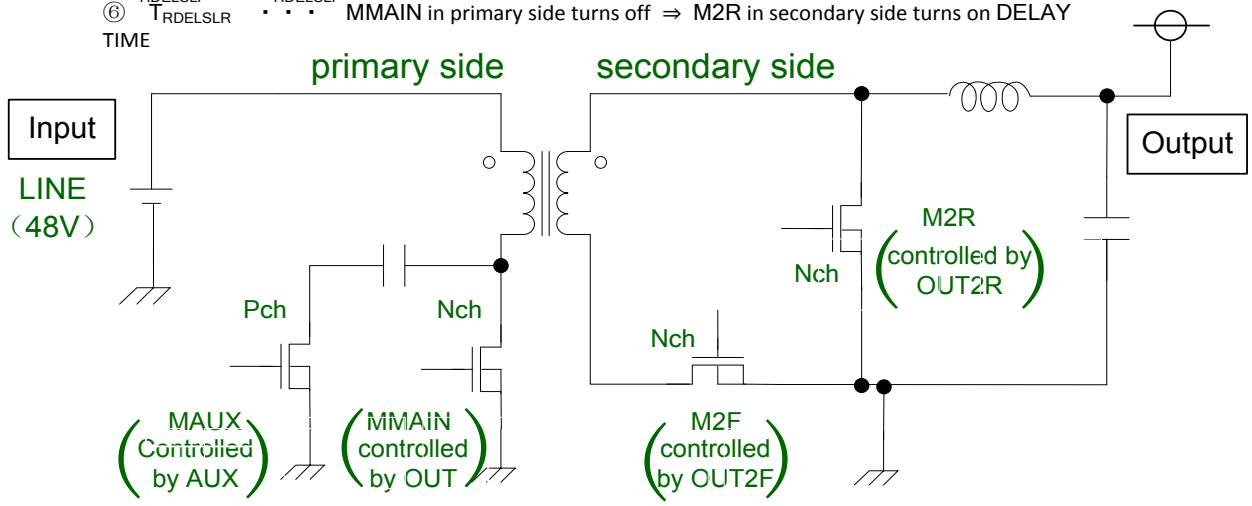
● **Adjustable Timing Through External Resistor**



∗ The times above are under the condition:
RTON=RTOFF=RDELON=RDELOFF1=RDELOFF2=RDELSLF=RDELSLR=120kΩ

■ **Adjustable timing by external resistor**

① T_{PERIOD} ・・・ PWM frequency. Time ① can be adjusted by RRTON, RRTOFF
② T_{RDELON} ・・・ M2R in secondary side turns off ⇒ MMAIN in primary side turns on DELAY TIME(T_{RDELON}´ and T_{RDELON} are linked）
③ $T_{RDELOFF1}$ ・・・ M2R in secondary side turns off ⇒ MAUX in primary side turns off DELAY TIME
④ $T_{RDELOFF2}$ ・・・ MMAIN in primary side turns off ⇒ MAUX in primary side turns on DELAY TIME
⑤ $T_{RDELSLF}$ ・・・ M2R in secondary side turns off ⇒ M2F in secondary side turns on DELAY TIME
（$T_{RDELSLF}$´ and $T_{RDELSLF}$ are linked）
⑥ $T_{RDELSLR}$ ・・・ MMAIN in primary side turns off ⇒ M2R in secondary side turns on DELAY TIME



●Typical Application Design

A forward converter application design is shown in Fig.31.Input Voltage ranges from 36~70V, output current from 0~8A and Output Voltage is 12V. The turns-ratio of main transformer is 1.5:1. Switching frequency is 310KHz, Max Duty is 66.6%. Regarding to over-current protection, CS1 and CS2 are all set to Io≒ 9A.

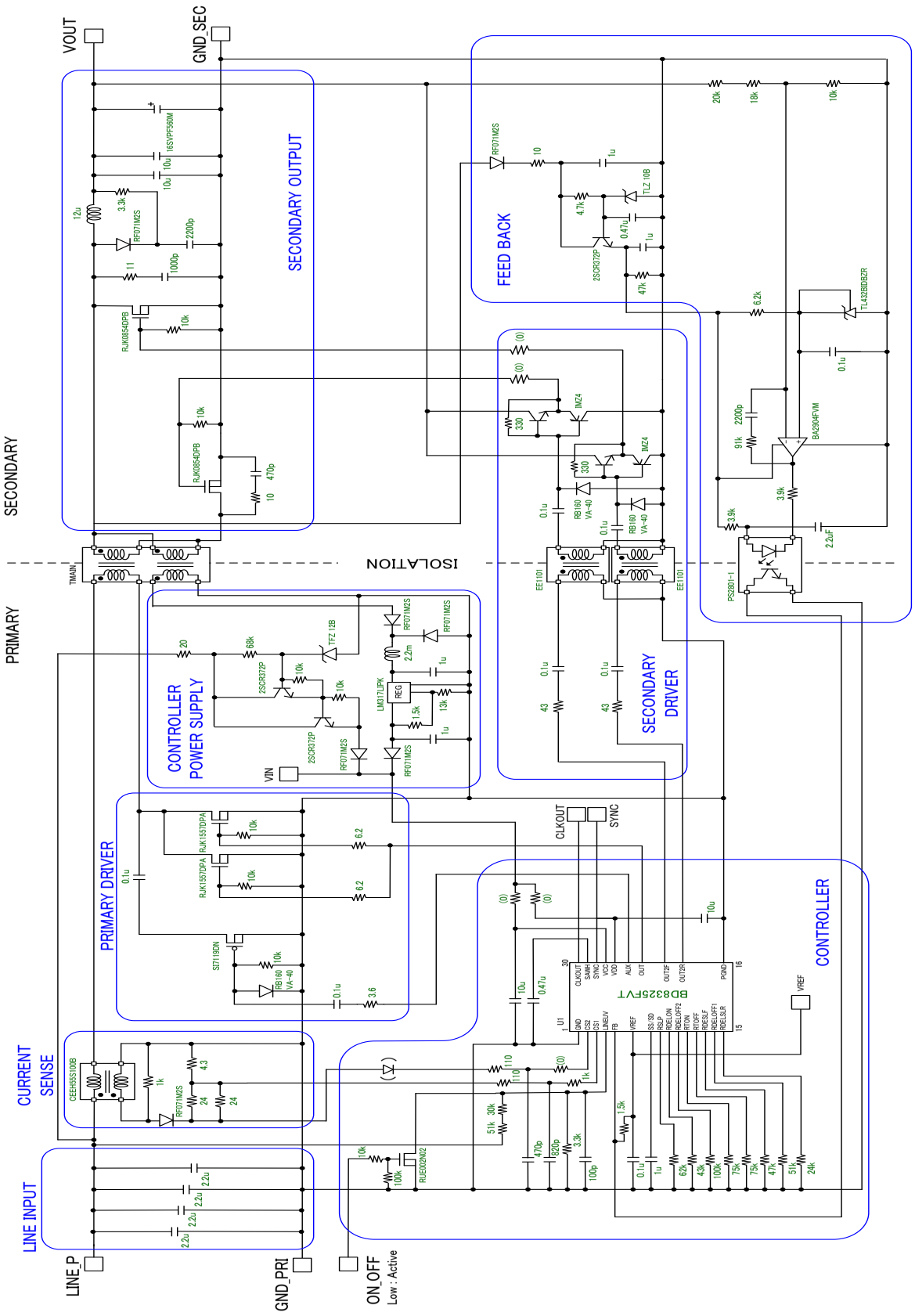


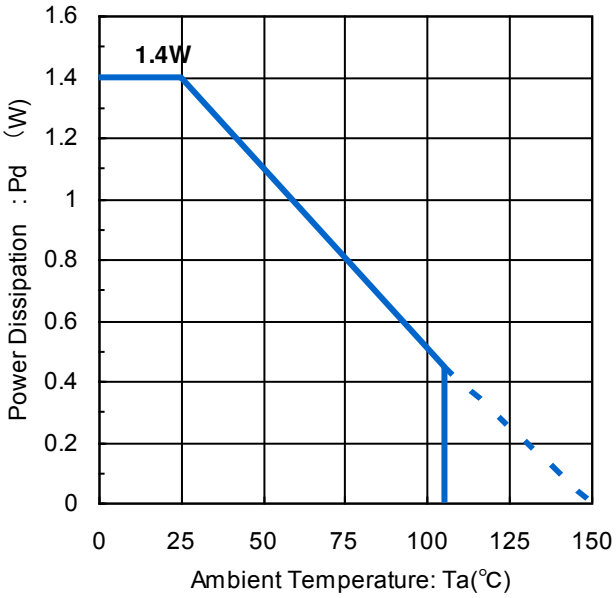
Fig.34 Application Circuit

●Power Dissipation

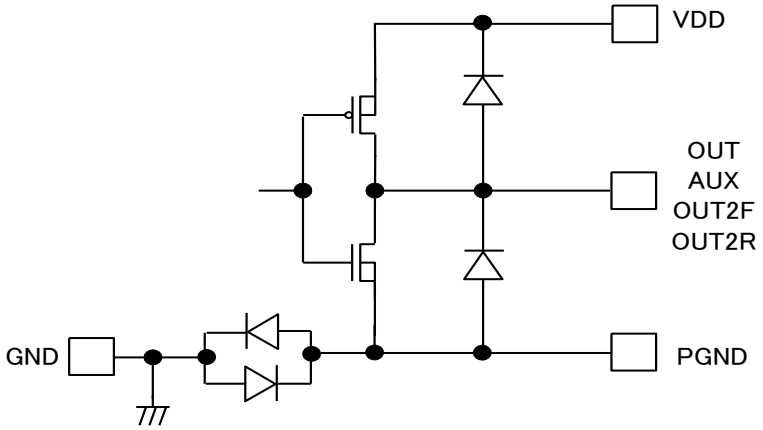
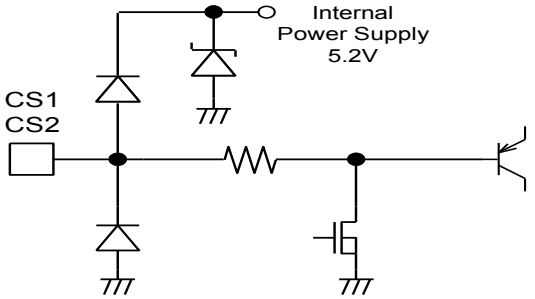
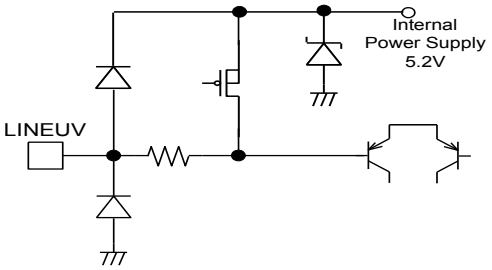
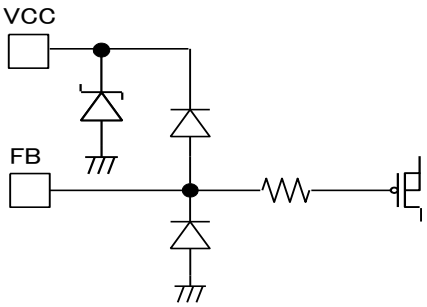
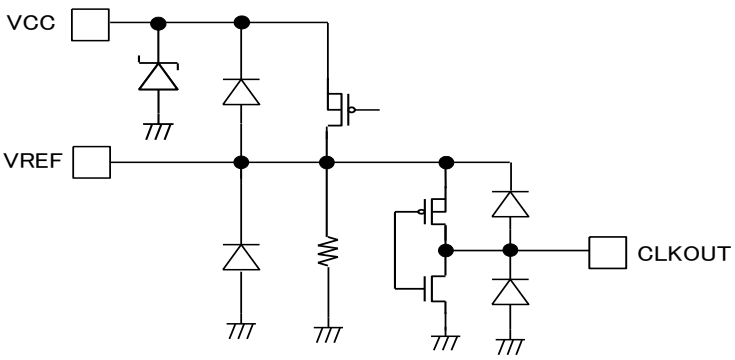
The thermal derating characteristic is shown below.
It is necessary to design the system requirements and board layout so that the junction temperature does not exceed 150℃.
In practical use, take into consideration that the temperature rise may likely to occur because of the heat dissipation of different PCB layout and other heat source.

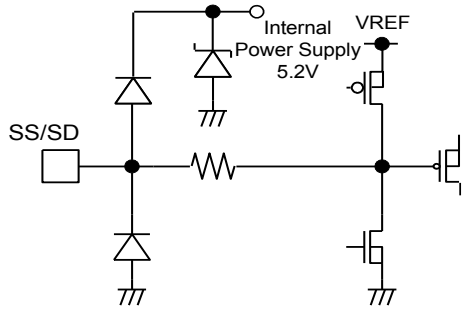
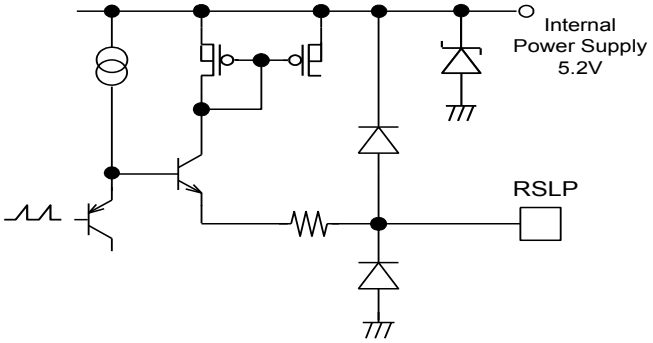
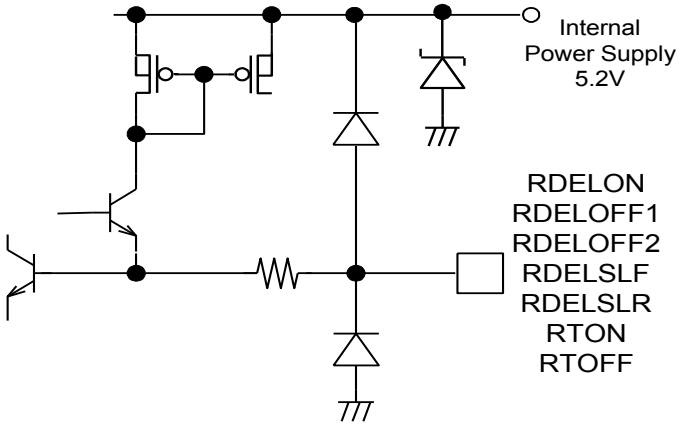
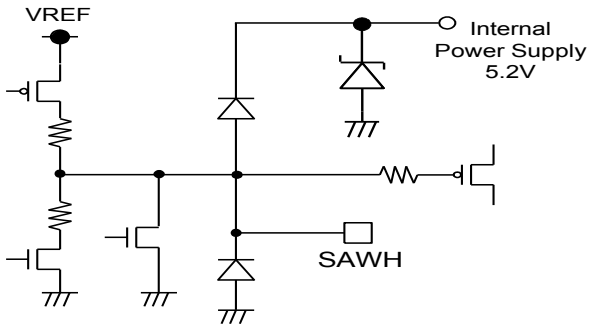
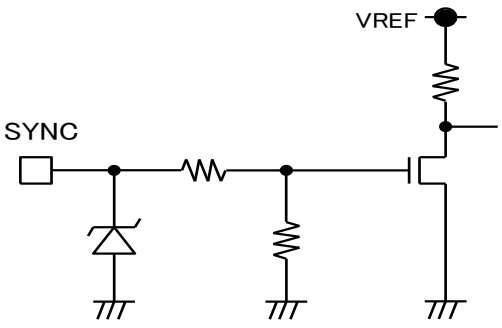
< PCB board >

FR4 (glass epoxy) substrate	:	114.3mm × 76.2mm × 1.6mmt
Copper foil surface	:	IC land pattern + test leads
2,3 layer, back side copper foil	:	74.2mm × 74.2mm



●I/O Equivalent Circuit

Pin No.	Pin Name	Pin Equivalent Circuit
1 16 18 20 22 24 26	GND PGND OUT2R OUT2F OUT AUX VDD	
2 3	CS2 CS1	
4	LINEUV	
5	FB	
6 27 30	VREF VCC CLKOUT	

Pin No.	Pin Name	Pin Equivalent Circuit
7	SS/SD	
8	RSLP	
9 10 11 12 13 14 15	RDELON RDELOFF2 RTON RTOFF RDELSLF RDELOFF1 RDELSLR	
28	SAWH	
27	SYNC	

●Operational Notes

1) Absolute Maximum Rating

Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

2) Power Supply Lines

Back EMF due to the output coil may result to a return current into the IC. Caution should be taken by putting capacitor between power supply and GND as a pathway for the return current. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors. If the connected power supply does not have sufficient current absorption capacity, the return current will cause the voltage on the power supply line to rise and may exceed the absolute maximum ratings. Therefore, it is important to consider circuit protection measures such as adding a voltage clamp diode between the power supply and GND pins.

3) GND potential

The potential of GND pin must be the lowest potential of all pins of the IC at all operating conditions. Ensure that no pins are at a potential below the ground pin at any time, even during transient condition. In particular, when the noise caused by the switching of OUT, AUX, OUT2F and OUT2R is big, please insert serial resistor to reduce the slew rate. As the output resistance of the IC is small, please contact ROHM for detailed information about the resistor to be inserted.

4) Heat Design

Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions

5) Pin Shorting and Incorrect Mounting

Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

6) Operation in Strong Magnetic Fields

Be mindful when operating in the presence of strong magnetic fields, as it may cause the IC to malfunction.

7) Capacitor between VREF and GND

The capacitor between VREF and GND should be above 0.1uF. For suppressing the noise and reducing the fluctuation on VREF line, please set the capacitor to appropriate value. Furthermore, VREF should not be open; otherwise the VREF output will be unstable.

8) Testing on application boards

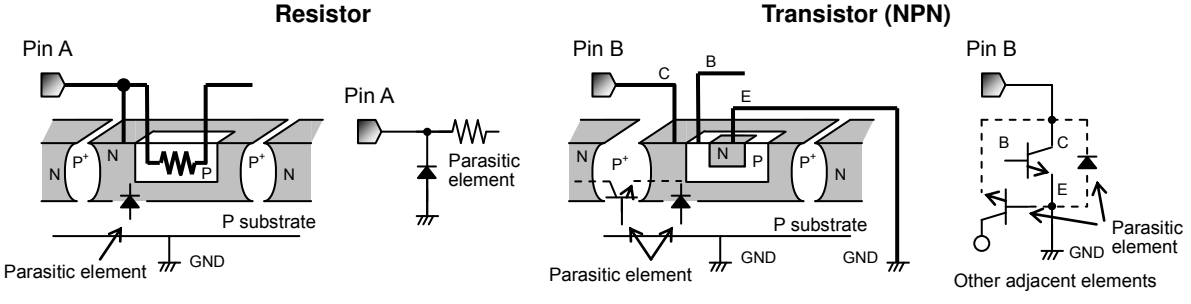
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from electro static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9) Input Pins

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of monolithic IC structure

10) Ground wiring pattern
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

11) Thermal shutdown circuit
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches a specified value. It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.

●Ordering part number

B	D	8	3	2	5	F	V	T	-	ME 2

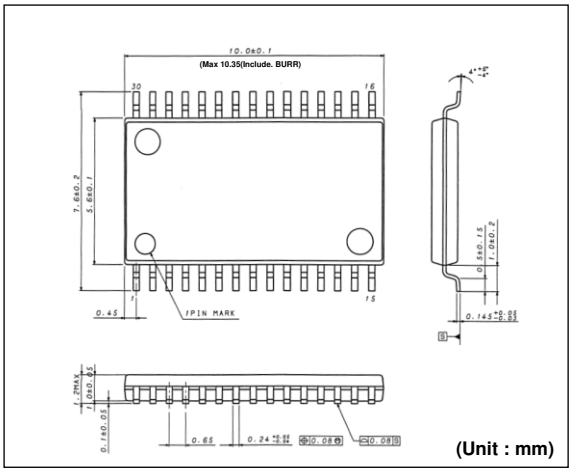
Parts. No

Package

Packaging and forming specification
E2: Embossed tape and reel

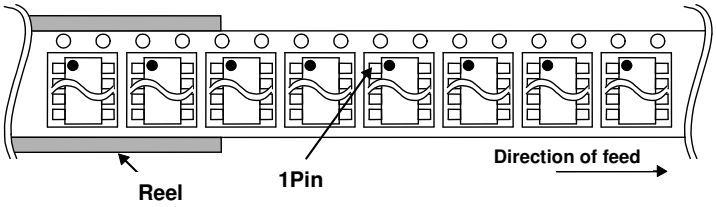
●Physical Dimension・Tape and Reel Information

TSSOP-B30

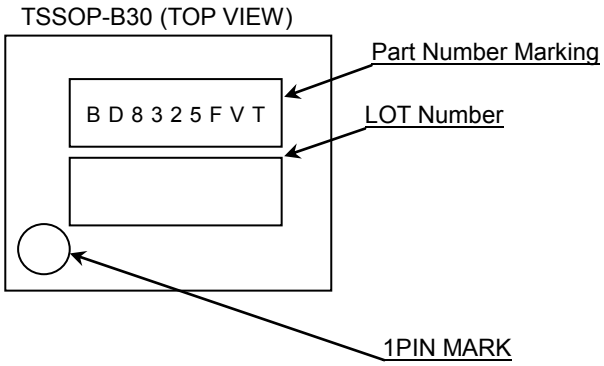


<Tape and Reel Information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The Direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



●Marking Diagram



Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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